DEVELOPMENT OF HIGH-THROUGHPUT NMR RF RECEIVER USING FPGA IP CORES

A Thesis

by

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MASTERS OF SCIENCE

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ABSTRACT

In NMR research, the signal acquisition instrument needs to fulfill high-speed, and high-throughput data collection. The modern NMR receivers are required to process signals through multiple-channels leveraging Software Defined Radio (SDR) logics. In order to support large amount of data inputs utilizing multiple channels, the device needs to speedily handle stream of input data within device's Onboard memory (RAM) and construct non-overflowing buffer to ensure flawless data transfer from analog-to-digital convertor (ADC). Parallel data handling techniques in FPGA is an essential component for NMR applications, because multiple process engine in FPGA digital logic ensures high processing speed. Direct-Memory-Access (DMA) function implemented in FPGA would greatly improve the data transfer rate. This would allow the NMR receiver to operate the system in real-time.

In this research work, we investigate a method to utilize the FPGA's Digital Down Conversion (DDC) logic to control the data flow in a versatile way. Furthermore, we examine methods in acquisition software to thoroughly access implemented FPGA logics utilizing LabVIEW software. Throughout this research, we investigate a software design pattern that would maximize its performance in parallel processing. Software architecture such state-machine, and Actor Framework would be examined to organize the device APIs.

DEDICATION

I dedicate this work to my parents.

ACKNOWLEDGEMENTS

I would like to thank my committee chair. Dr. Steven M. Wright and my committee members Dr. Jim Ji, Dr. Mary McDougall, and Dr. Hangue Park for providing great mentorship and guidance throughout the course of this research. I would also like to express my very great appreciation to my friends and colleagues and the department faculty and staff for making my time at Texas A&M an excellent experience.

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Contributors

This work was supervised by a thesis committee consisting of professors Steven M. Wright [advisor], Jim Ji, Hangue park of the Department of Electrical & Computer Engineering and professor Mary P. McDougall of the Department of Biomedical Engineering.

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NOMENCLATURE

API	Application Programming Interface
A/DC	Analog/Digital Converter
DDC	Digital Down Conversion
DMA	Direct Memory Access
DLL	Dynamic Link Library
FID	Free Induction Decay
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
IF	Intermediate Frequency
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LO	Local Oscillator
MRS	Magnetic Resonance Spectroscopy
MRI	Magnetic Resonance Imaging
NMR	Nuclear Magnetic Resonance
RAM	Random Access Memory
RF	Radio Frequency
SDR	Software Defined Radio
VCXO	Voltage-Controlled Crystal Oscillator

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1. INTRODUCTION

1.1 Background

Magnetic Resonance System Lab (MRSL) at Texas A&M university make use of 4.7 Tesla, 33cm superconducting magnet, and 40cm horizontal bore magnet driven by Varian's super-heterodyne transceiver system. The facility also employs triple-tuned coil for multi-nuclei spectroscopy facilitated by broadband system composed of Ultraview AD-16-250, high-speed RF receiver and, NI PCIe-6323, RF & gradient waveform generator.

There has been ongoing research in MRSL to develop enhanced RF signal receiver to support NMR application that utilizes multiple phased array coils. One of the core objective in MRSL is to optimize the broadband RF receiver to perform NMR signal acquisition in higher-fields strength with multiple frequency bands.

The current broadband receiver in MRSL integrated with Ultraview AD-16-250, facilitates MR signal acquisition in wideband utilizing direct-sampling method. The device is capable of digitizing sample up to 250MS/S. The board is capable of transporting the sampled data through PCI-express bus to store the digitized samples in host computer.

One of the shortcomings in current broadband system exist with the fact that the continuous acquisition with long echo time and short repetition time is not achievable. This is due to the limitation in data throughput. As part of MRSL effort to develop broadband receiver capable of capturing signals with continuous data streams, the investigation of FPGA based data acquisition system has led us to implement digital down conversion logics into the RF receiver. Pentek 78862, signal acquisition card leverages FPGA digital down conversion IP core to decimate the

signal during its data transfer process. The digital down conversion (DDC) core allows the system to define eight independent software-defined FIR filters in a single acquisition channel to facilitate data reduction during data transferring process to the host PC.

1.2 Research Motivation and Objectives

In many magnetic resonance applications, NMR receivers are becoming important part of the system because the use of higher field strength is common to many commercial MRI/MRS equipment . The evolution of RF coil designing techniques has led NMR receivers to accept signals in much higher frequencies. It is a major challenge to design broadband NMR receiver to capture wide range of RF signals, because NMR broadband application requires the signal acquisition device to digitize samples at much higher sampling rate to meet the Nyquist criterion.

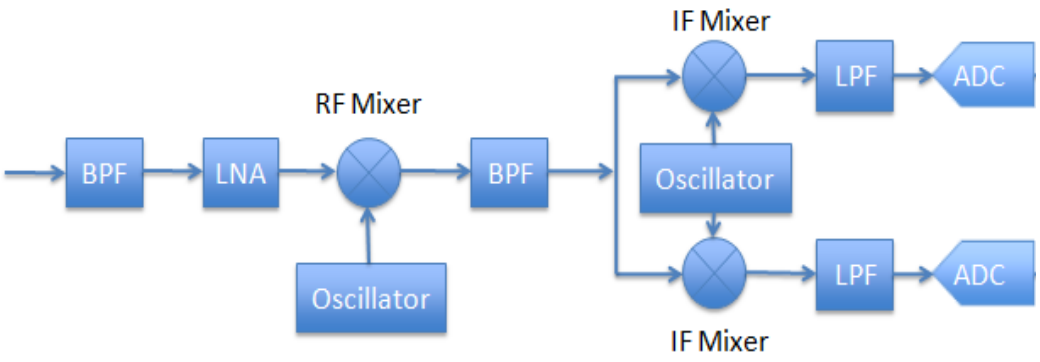


Figure 1 Heterodyne RF Receiver

In order to overcome these challenges, heterodyne receiver design is utilized to translate the RF signal down to a Intermediate Frequency (IF) to allow the ADC to configure its sampling

frequency in much lower settings. The multiple mixed down stages operating with dedicated local oscillator allocates specified intermediate frequency. This process translates high-frequency MR signal close the baseband to provide more leeway in digitization rate for ADC.

The 4.7 Tesla, 33cm superconducting magnet, and 40cm horizontal bore magnet driven by Varian's transceiver utilizes super-heterodyne structure. The multi-stage heterodyne architecture allows the Nyquist sampling frequency to be set at 50kHz. The Varian generates less sample points compared to systems that uses the direct sampling method like Ultraview AD-16-250.

Direct-sampling RF receiver (Non-Heterodyne) design requires the A/DC to digitize data in much higher rate. The common drawback of using direct-sampling method comes with the fact that large amount of data needs to be buffered in limited memory space. The digitized data needs to be fetched in speedily manner to avoid overflowing the memory space. The use of integrated FPGA digital down conversion logic assures the high-speed data transport. DDC core handles data reduction utilizing decimation logic associated with software FIR filter.

The usage of FPGA in digitizer could accomplish high-speed data transfer rate utilizing technique such as direct memory access (DMA). Digital Down Conversion (DDC) can make use of the real-time decimation function to handle large input data stream from multiple array coils. Incorporating FPGA with direct sampling digitizer provides numerous advantages over the simple heterodyne system with regard to the data processing speed. The software tunable FIR filters implemented in FPGA allows the system to contract the large amount of data.

Building digital processing logics (FIR filter, Decimator, and Local Oscillator) in FPGA is more advantageous than integrating the signal processing logics in hardware components. It is

common to see in modern signal receivers to incorporate digital signal processing unit to be developed in software. Super-heterodyne logic components (anti-aliasing filters, and band pass filter ,mixers, and oscillators) can be configured in FPGA to translate RF signal into a baseband. This allows the system to be more adaptable and flexible.

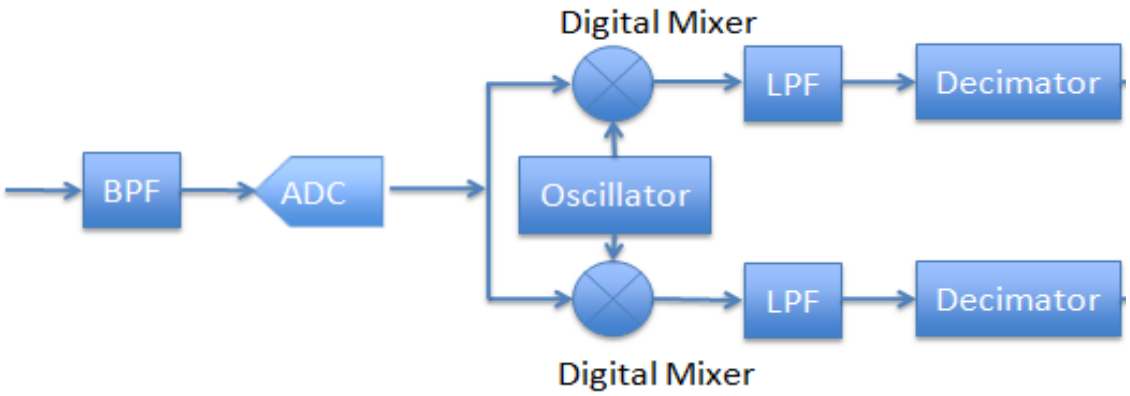


Figure 2 Direct-sampling with FPGA DDC Core

The FPGA DDC core could be set to have multiple sub-channels define by the FIR filters to capture a wideband of RF signals. Digital down conversion core logic is an essential component for broadband NMR receiver system. FIR filter bandwidth is reconfigurable through API settings and the tunable local oscillator (LO) facilitate FPGA logic to select the frequency band define by local oscillator frequency in the software. When DDC Cores are simultaneously operating through parallel DDC processing unit, the FIR filter can be tuned independently to monitor multiple channel band. The multi-channel DDC core accomplishes NMR receiver to examine multiple nuclei spectrum through single data acquisition channel.

For Magnetic Resonance Imaging (MRI), and Magnetic Resonance Spectroscopy (MRS) simultaneous broadband signal acquisition can be further extended to support addition RF

acquisition channels to achieve parallel data collection. The usage of multiple acquisition channels would led the device to handle even more sample points.

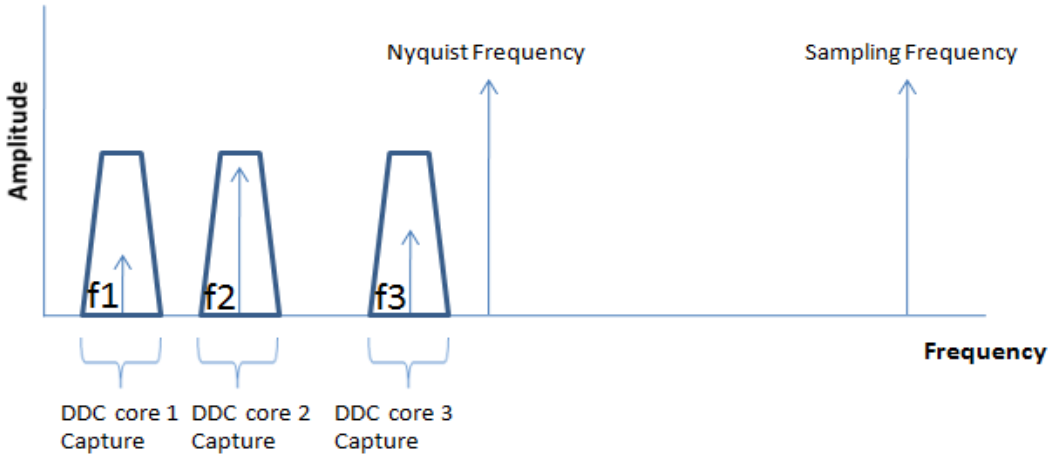


Figure 3 Broadband Signal Capture with parallel DDC Core

The direct-sampling receiver is configured with high-digitizing rate to meet Nyquist criterion. Due to the fast sample generating speed, the large data stream needs to be handled by the decimation function in DDC core. The signal acquisition instrument needs to fulfill high-speed, and high-throughput data collection in NMR experiments. NMR receivers are required to acquire signals in multiple-channels to support experiments. In order to support large amount of data inputs, the instrument needs to speedily handle stream of input data within device's Onboard memory (RAM). The device needs to construct non-overflowing buffer to ensure flawless data transfer from analog-to-digital convertor (A/DC). Parallel data processing is an essential component for NMR applications, because multiple process engine in FPGA's digital logic gate ensures high processing speed. Direct-Memory-Access (DMA) function implemented in FPGA would greatly improve the data transmitting process to allow the NMR receiver to operate the system in real-time.

2. HARDWARE OF BROADBAND RECEIVER

2.1 Signal Acquisition Card Overview

In MRSL, Ultraview AD-16-250, digitizer card is integrated as part of the RF receiver system to support broadband NMR signal acquisition. The device features Xilinx Kintex FPGA chip to support fast data transferring process through direct memory access (DMA) capability. However, the Ultraview AD-16-250 does not feature built in digital down conversion (DDC) core in FPGA which would execute decimation and multiple channel selection.

In the other hand, Pentek 78862 has FPGA DDC core to support variable controlled FIR filter logic and decimation logic along with direct memory access function to customize software define radio (SDR) component. In this research, the objective is to utilize Pentek 78862 to validate parallel DDC core execution in data acquisition to enhance data throughput for NMR application which can handle to acquire multiple nuclei in wide range of frequency spectrum.

Pentek's Jade™ family Model 78862 is a multi-channel high speed digitizer that features impendent SDR component for each acquisition channel. The device includes four 200-MHz, 16- bit analog to digital converters. Xilinx® Kintex® UltraScale™ FPGA (Field−Programmable Gate Array) contains four independent multiband DDC FPGA IP core to support 8 narrowband sub-channels. 5GB of DDR4 RAM provides a memory space to create circular buffer in the data transferring process. The data bus utilizes backward compatible PCI-express bus to support 8 lane of data transferring channels. The clock synthesize features programmable voltage control oscillator to provide different sampling speed and synchronization clock rate.

2.2 Device Architecture

The frontend of the device is composed of four independent 16 bit resolution analog to digital convertors, Synchronization Gates, and Clock synthesizer. The Kintex FPGA digital signal processing unit provide software defined radio (SDR) components (mixer, numerical control oscillator, IQ formatter, sub-channel configuration unit) . Each of the SDR component are control by registry assignments through bit allocation in the control APIs. The control API maps specific command to a pre-allocated memory address to programmatically control the digital signal processing core.

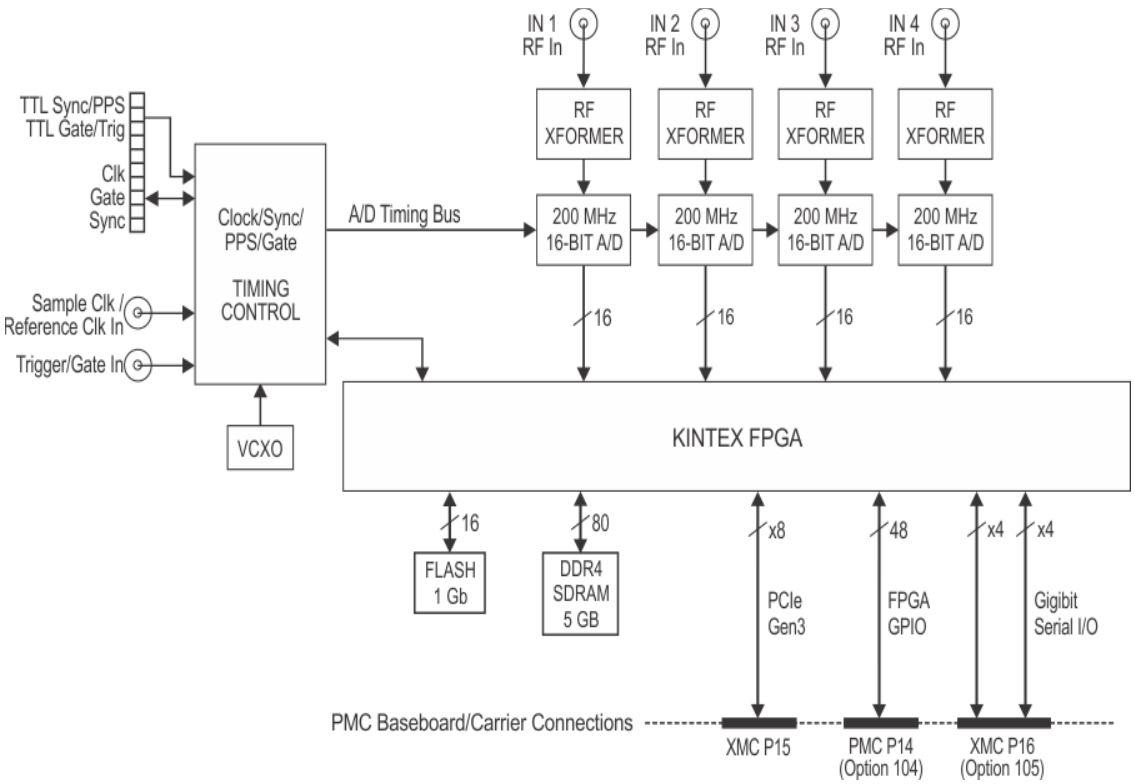


Figure 4 Pentek's Jade™ family Model 78862 Device Architecture

Figure source : Pentek's Jade™ family Model 78862 User Manual

2.3 Signal Resolution

Signal Resolution is define by the number of bits supported by A/D converter. In NMR applications, it is critical to capture signal with narrow resolution to differentiate noise level over a small NMR signal. The strength of the magnetic field provides a proportional improvement of the NMR signal. Operating NMR signals in low magnetic field, the signal to noise ratio (SNR) decays proportionally and narrow resolution step width is required to digitize echo signal without any distortion.

The resolution step width is determine mainly by the device input range and resolution bit. The A/D convertor takes an NMR echo signal and transforms it to a binary number. The binary number digitized in signal receiver represents a specific electrical signal level in voltage. Pentek's Jade™ family Model 78862 specifies resolution bit of 16. This represents 2^{16} ,65,536 signal levels. The total number of binary level accessible based on bit resolution is $2^{\text{Resolution bit}}$,while it can range its binary combination from (00000000/00000001) = 1 level to (11111111/11111111) =65536 levels.

16 bit Binary Representation	8 bit Binary Representation
0000/0000/0000/0001 = 1	0000/0001 = 1
0000/0000/0000/0010 = 2	0000/0010 = 2
0000/0000/0000/0011 = 3	0000/0011 = 3
.	.
.	.
.	.
1111/1111/1111/1101 = 65533	1111/1101 = 253
1111/1111/1111/1110 = 65534	1111/1110 =254
1111/1111/1111/1111 = 65535	1111/1111 = 255
Total =65536 level	Total = 256 level

Figure 5 Number of levels represented by 16 bit, 8 bit resolution

The resolution step width is define by number of available level define by the resolution bit and device input range. Pentek's Jade™ family Model 78862 specifies its maximum, and minimum input level by 0.719V, and -0.719 respectively. The total device input range is 0.719V - (-0.719v) = 1.439V. Resolution step width is the smallest change in signal that the device can perceive. The resolution step width can be expressed as the following.

$$\begin{aligned}\text{Resolution step width} &= (\text{ Input range / Number of available levels }) \\ &= (\text{ Max Limit - Min Limit}) / 2^{\text{Resolution bit}} \quad) \\ &= (\ 0.719 - (-0.719)\ ) / 2^{16} \\ &= 1.439 / 65{,}536 \\ &= 26.95\ \mu V\end{aligned}$$

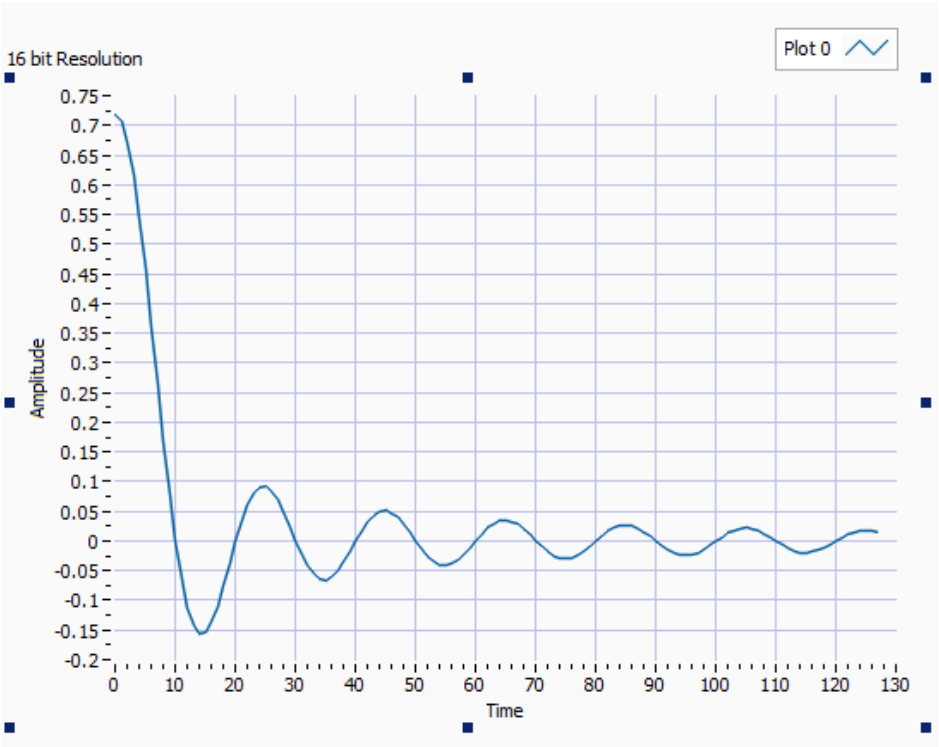


Figure 6 SINC waveform (FID) with 16 bit resolution capture

Using the same range defined by maximum, and minimum input level of 0.719V, and -0.719 respectively, the 8 bit resolution signal capture can distort waveform information due to larger code width.

$$\text{Resolution step width} = (\text{Input range} / \text{Number of available levels})$$
$$= (\text{Max Limit} - \text{Min Limit}) / 2^{\text{Resolution bit}})$$
$$= (0.719 - (-0.719)) / 2^{8}$$
$$= 1.439 / 256$$
$$= 5621.09\ \mu V$$

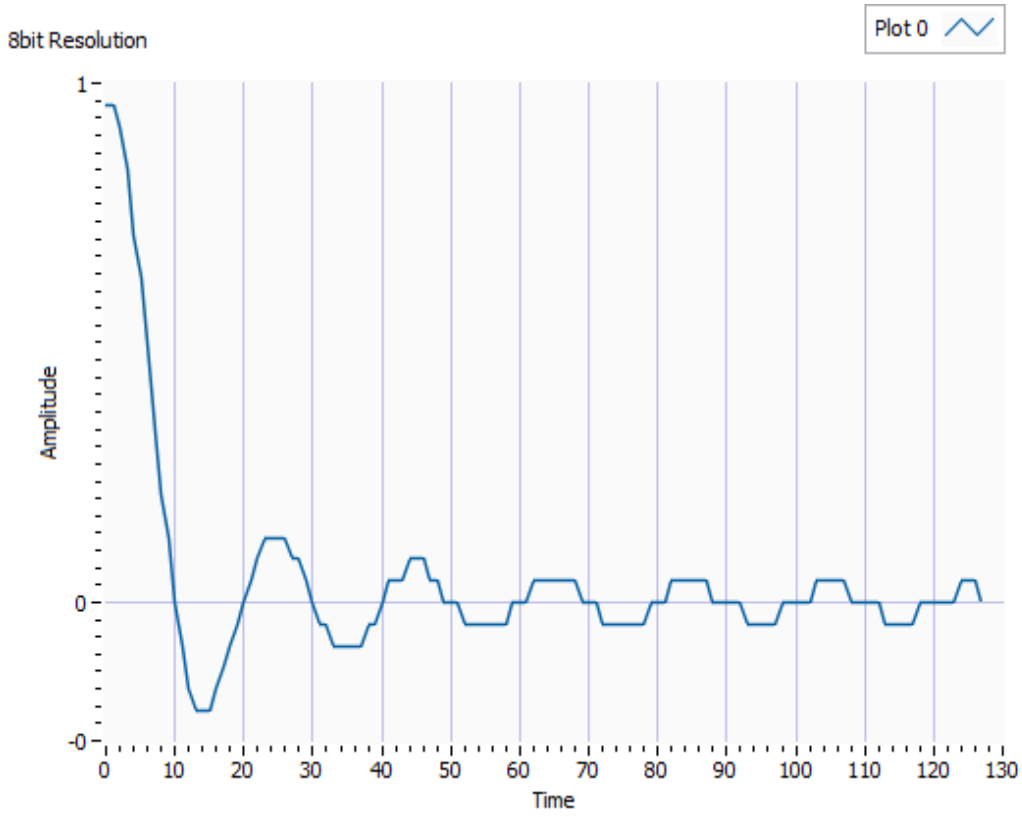


Figure 7 SINC waveform (FID) with 8 bit resolution capture

2.4 Digital Trigger

NMR signal receiver requires to consist digital triggering function to synchronize the signal acquisition duration along with the frequency encoding duration. Pentek's Jade™ family Model 78862 provides digital start trigger function to initiate the sampling clock to digitize discrete number of sample points.

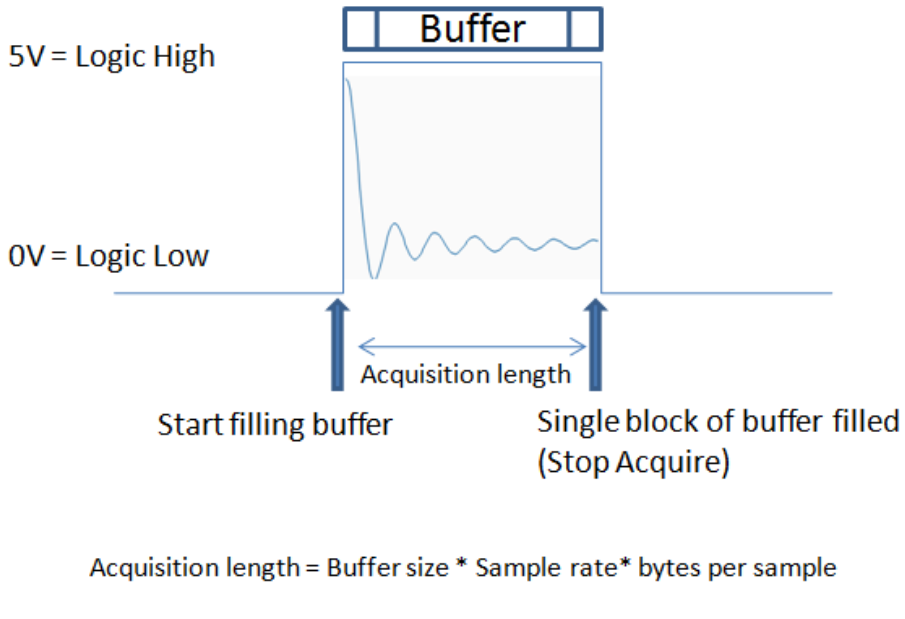


Figure 8 Digital Trigger for a single echo capture

The type of trigger function supported by Pentek's Jade™ family Model 78862 is a digital TTL trigger. The trigger operates with two binary discrete levels. The transistor to transistor logic (TTL) follows two logic states: low state and high state. The transition between the low states to high state is what defines the acquisition start time reference of the signal capturing process. The Pentek 78862 model defines the starting reference provided from the external digital TTL signal and the logic transition point is when the buffer starts transporting data from the A/D convertor.

2.5 Sampling Clock & Reference Clock

Pentek's Jade™ family Model 78862 derives sampling from the board clock rating at 250 MHz. The 250MHz On-board clock is synthesized by a clock derivation process in FPGA to derive 200MHz data sampling clock to provide A/D conversion period. The device is capable of deriving its 10MHz reference clock from the 250MHz on-board clock. In NMR signal acquisition process, an accurate 10MHz external clock is utilized to achieve phased loop lock (PLL). In NMR system, the signal generator and signal receiver use identical reference clock source to synchronize the RF transmit signal and RF receiver signal. The 10MHz sinusoidal sine signal is generated with crystal oscillator for synchronization.

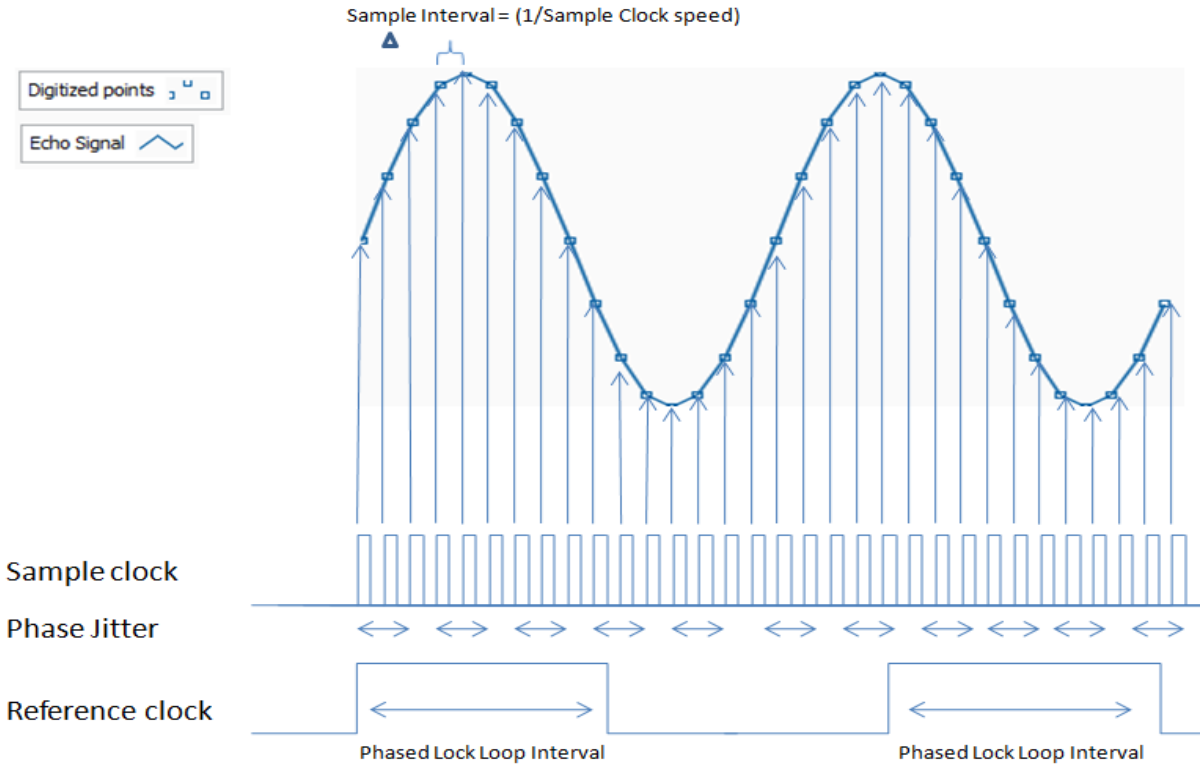


Figure 9 Sample Clock and PLL reference

Sampling clock utilizes digital TTL (transistor to transistor logic) to digitize analog signal in to a binary representation during its logic transition. At each recursive digital edge, an analog sample point is converted to a digital binary format. Four independent acquisition channel has its own A/D converter that supports 200MHz sampling rate derived by the on-board clock.

2.6 Data Throughput & PCI express BUS

The main objective of this research is to provide continuous data transfer to support acquisition with high Nyquist sampling frequency. It is important to have a maximum data transport bandwidth between the acquisition software, and the data buffer to optimize abundant amount of data being digitized through multiple channels.

Pentek's Jade™ family Model 78862 interfaces PCI-express Bus to support high transfer rate. This allows the system to continuously stream the data from a 5GB of DDR4 RAM to a host PC's disk space. The device encounters maximum input flow of 1.6GB/Second when all four channel is configured with the maximum sampling rate of 200MS/s.

Maximum Input flow = (Sample Rate * Number of Channels * Number of bits per Sample)

= (200MS/s) * 4 * 16bit

= (800MS/s) * 16 bit/sample

= (800MS/s) *2 Byte/sample

= 1.6GB / second

The system needs interface appropriate data bus to generate corresponding output stream from the buffer to avoid overflowing the memory space. Pentek's Jade™ family Model 78862 can be configured with PCI-express bus. The PCIe bus is backward compatible to utilize different number of lanes(x1, x4, or x8). Each PCI-express lane supports 250MB/S of transfer rate. 8 lanes of bus link supports up to 2GB/s of data throughput bandwidth.

2.7 Buffered Data Stream

The main purpose of this research is to provide continuous data transfer to handle high-frequency signal acquisition. It is important to have a maximum data transport bandwidth between the acquisition software and data buffer to optimize abundant amount of data being digitized in multiple channels. A buffer is considered as a temporary storage in device memory for digitized samples. The data storage is reserved in 5GB of DDR4 of on-board memory and it allocates a space to stream binary data through direct memory access (DMA).

At the stage of direct memory access (DMA) data transferring , binary samples are collected through the A/D convertor to be placed initially in the FIFO memory space. The FPGA DDC data socket arranges the data transfer through the PCI-express bus to allocate another reserved memory space inside the PC RAM. The Navigator Board Support Package (BSP) can build software acquisition application in C++ / LabVIEW to fetch the data out from the specified memory address in PC RAM. LabVIEW can hold up to 2GB of data in its application memory.

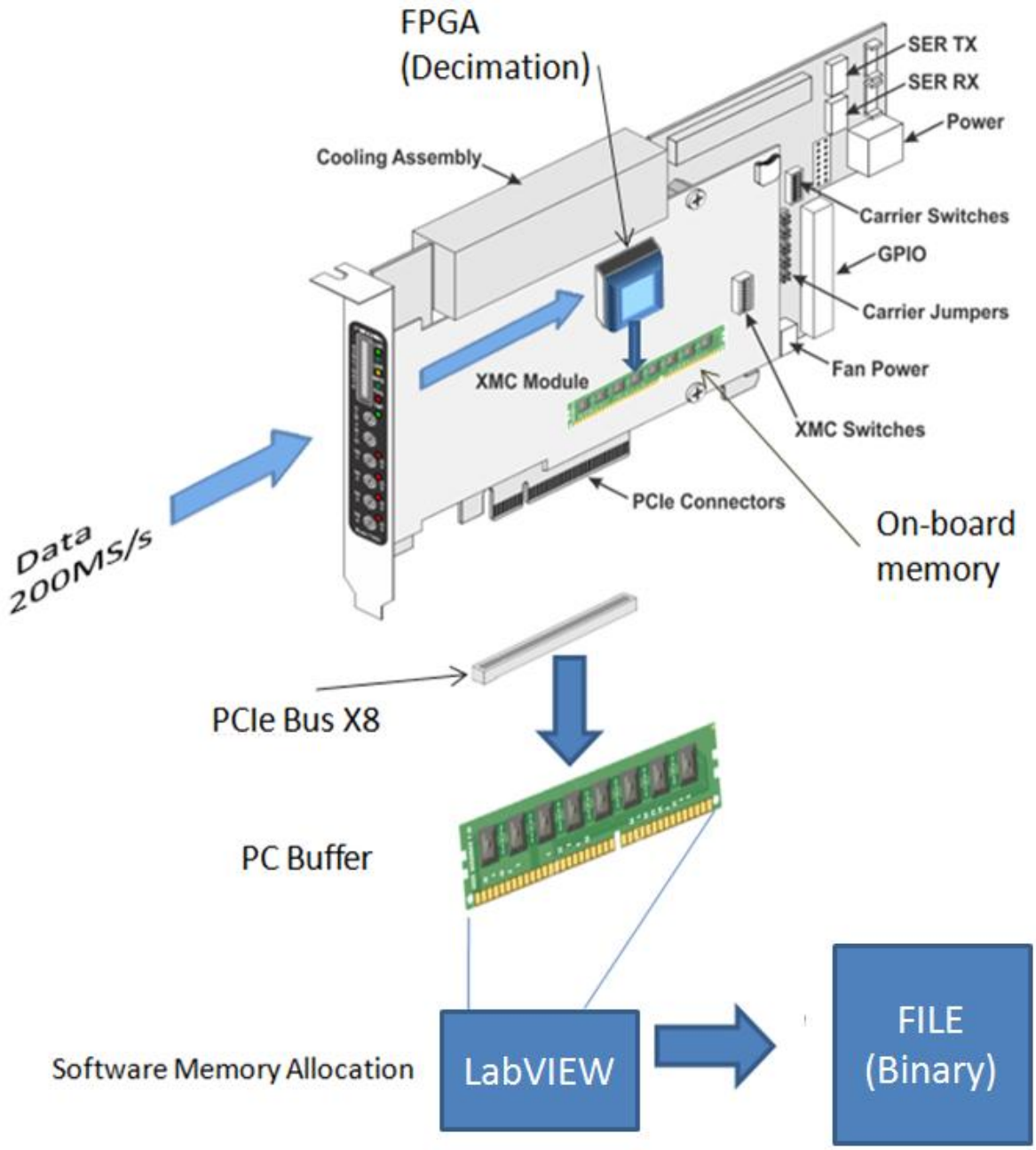


Figure 10 Data stream architecture

When transferring data from the receiver board to the PC RAM the system depends on the PCI-express bus bandwidth (250MBytes/second) per lane. If the data arrival speed is faster than the speed of data being transferred out through the PCI-express bus, the buffer would be overwritten

by the incoming stream. The larger the buffer memory size, the system less dependent on the transferring bandwidth. The device seizes more data while remaining data are waiting to be fetch to the PC RAM. The acquisition engine pre-allocates memory space in PC buffer and records data in real-time in to the disk. Signed 16 bit integer representation is configured to store single sample as a 2 Byte binary data. DDC core operating in FPGA would control the amount of data flow utilizing decimation function. FIR filter bandwidth configured in DDC core facilitates the reduction in size of the data stream. In order to avoid data from being overwritten by the incoming data stream, the sampled data needs to be fetched out of from the buffer much in faster rate.

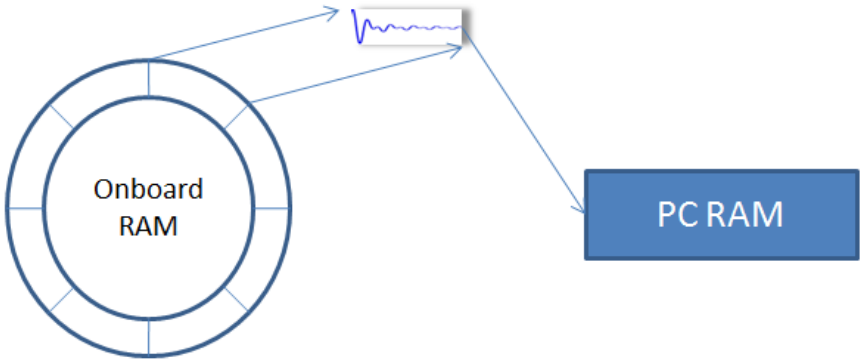


Figure 11 Circular Buffer

Direct Memory Access (DMA) function in FPGA would ensure the buffer to fetch the data in speedily manner to prevent the memory space from being filled up by incoming data streams. The FPGA core utilizes this DMA function referencing its cycle with 40MHz Time base clock. This would allow the system to fully make use of bandwidth of PCI-Express bus. Circular buffer would allow the receiver to operate acquisition continuously through re-allocating the buffer space that has been already allocated in prior DMA process.

3. NMR SIGNAL ACQUISITION METHODS AND TECHNIQUES

3.1 Software Defined Radio

Legacy RF receiver system implements its signal processing component in hardware (e.g. decimators, mixers, IQ modulators, amplifiers, band-pass filters). The components like amplifier and band-pass filter provides only fixed point adjustment for hardware based RF receivers. These hardware defined RF system deals signal processing in analog fashion. Reconfiguring different settings to adapt wide variety NMR application is rather complex in these hardware defined radio system. Analog filters has limitation in achieving wide range of gains. Also it is difficult to design a band pass filter that would collect signal in every possible frequency band that is allowed by Nyquist Frequency.

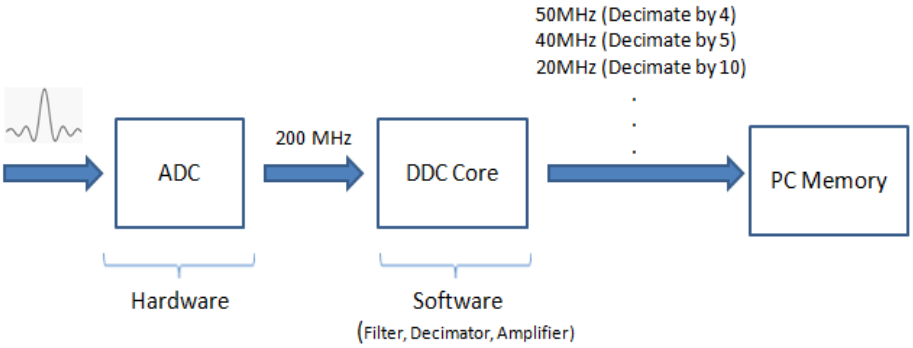


Figure 12 RF receiver with SDR

The software defined radio system seeks to substitute as much of the complex analog hardware based signal processing implementation into a digital processing component like FPGA. Implementing digital signal processing logic blocks in FPGA allows to implement decimators, mixers, IQ modulators, amplifiers, and band-pass filters in digital fashion. The benefit of

implementing signal processing unit in digital fashion lies with the fact that processing unit is fully reconfigurable through simple changes in software parameter. The gain control of the amplifier, bandwidth selection of the filters, frequency assortment of the mixer, factor of decimation in FIR filter are controlled in digital domain. This provides adaptable software processing block to simply the old-fashion analog controlled RF receiver into a computerized processing unit.

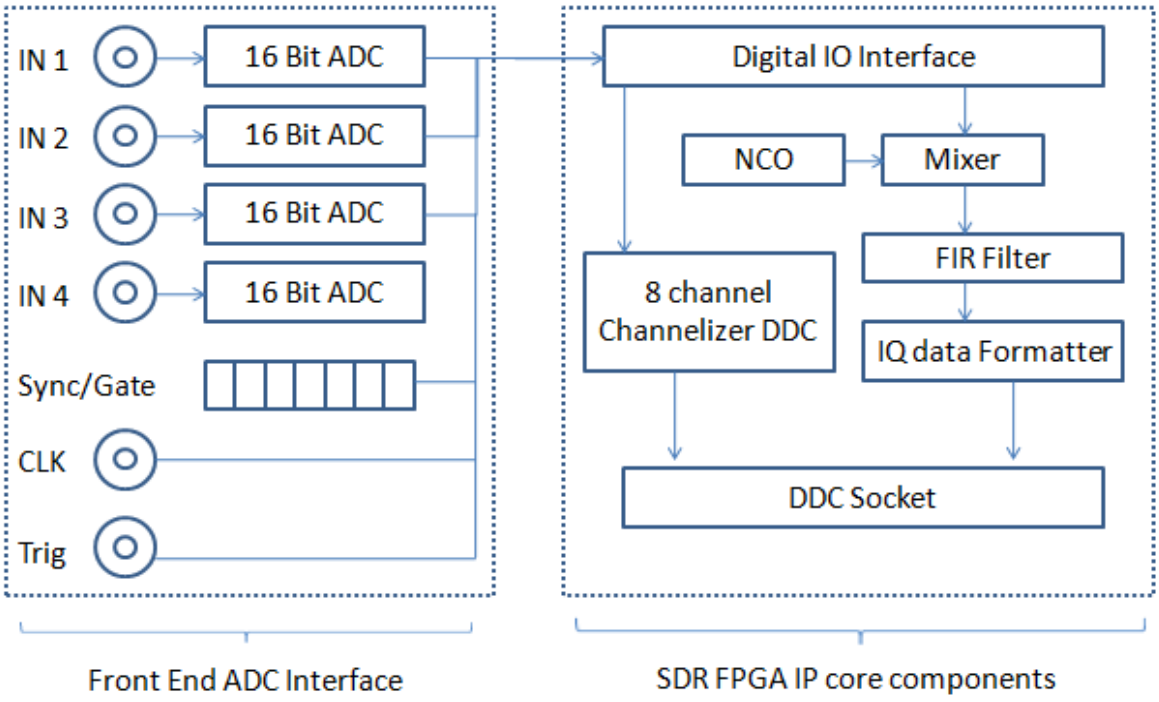


Figure 13 ADC front-end & SDR components

The Pentek 78862 takes software define radio approach in its signal processing architecture to achieve high- throughput, multi-channel wideband RF signal capture. Digital Down Conversion unit operates its FPGA logic to perform frequency translation into IF band with software controlled oscillator. FIR filter bandwidth can be straightforwardly tuned with decimation, and

the sample rate settings in A/D convertor. The convenience of using DDC core in FPGA lies with the fact the system can be configure to preselect signal of interest and neglect all other signal by adjusting the local oscillator (LO) frequency. The fact that system can create parallel DDC core processor in a single channel allows the user to achieve multi-narrow band signal capture. Multiple sub-channel acquisition in Pentek 78862 make use of the parallel independent DDC core leveraging software define narrow band filters. Pentek 78862 utilizes 80 percent of the sampling rate to allocate the FIR filter bandwidth. It reduces the bandwidth even further with the decimation factor controlled by the software.

3.2 Sequential Triggering Acquisition

RF acquisition process relies on the onboard memory to make recursive data transfer from A/D convertor to a PC memory space. The size of the buffer determines the number of iterative data filling action when the input data stream is much greater compared to the data being fetched out of the buffer. The digitized sample transfers through an onboard memory space facilitate by FIFO stream queue. The data sample is transferred making use of the direct memory access (DMA). In NMR application, short repetition time (TR) is typically implemented in gradient echo pulse sequence to assure fast processing speed. Lengthy echo acquisition time (TE) is required to achieve enhanced spectroscopy results. Utilizing narrow filter bandwidth and high sampling rate improves the spectral resolution in FFT process. The number of buffer blocks filled in each trigger event determines number of acquisition iteration steps allowed by the total memory size of the buffer. Pentek 77862 allocates the queuing memory space based on the number of triggered buffer blocks. And the size of the individual buffer blocks are predefine

based on the echo acquisition time. Total memory space enable by buffer setting in software is followed by the expression bellow. When signal acquisition is driven with sequential trigger, a buffer block size is what defines the duration of echo time. It is typical to capture 64, 128, 256, and 512 echoes to construct K-space when performing image reconstruction. The number of buffer blocks has to match the number of phase encoding steps, since the size of individual buffer block determines the acquisition duration.

Occupied on-board memory space = (Number of buffer blocks) * (Buffer size)
5GB On-board memory = (64 Phase Encoding steps) * (Buffer size)
5GB On-board memory = (128 Phase Encoding steps) * (Buffer size)
5GB On-board memory = (256 Phase Encoding steps) * (Buffer size)
5GB On-board memory = (512 Phase Encoding steps) * (Buffer size)

Constructing a MRI pulse sequence with more phase encoding steps reduces the size of the individual buffer block, since the total on-board memory space is finite. Pentek 78862 has memory capacity of 5GB. Storing every digitized sample into a buffer for each triggered phase encoding iteration utilizes the maximum buffer size. Pulse sequence implemented with more phase encoding step results in smaller size of the buffer block.

Buffer size = (On-Board memory) / (Number of buffer blocks)
76MB ` = 5GB / (64 Phase Encoding steps)
39MB = 5GB / (128 Phase Encoding steps)
19MB = 5GB / (256 Phase Encoding steps)
9MB = 5GB / (512 Phase Encoding steps)

Considering maximum sample rate of 200MHz with 2 byte signed integer data representation, the maximum acquisition duration allowed for each triggered cycle computes to be the following.

Acquisition duration (TE)	= (Buffer size) / (Bytes per Sample) / (Sample rate)
0.19 seconds	= 76MB / (2 Byte) / 200MHz
0.0975 seconds	= 39MB / (2 Byte) / 200MHz
0.0475 seconds	= 19MB / (2 Byte) / 200MHz
0.0225 seconds	= 9MB / (2 Byte) / 200MHz

With different decimation factor, the system can lengthen the acquisition duration for the each echo acquisition at each phase encoding steps. The acquisition length of the echo increases accordingly with the decimation factor. If DDC core that sets decimation factor of 2, the acquisition length doubles.

Acquisition duration (TE) =	Buffer size / Bytes per Sample / Sample rate * Decimation
0.38 seconds	= 76MB / (2 Byte) / 200MHz * 2
0.195 seconds	= 39MB / (2 Byte) / 200MHz * 2
0.095 seconds	= 19MB / (2 Byte) / 200MHz * 2
0.045 seconds	= 9MB / (2 Byte) / 200MHz * 2

3.3 Circular Buffer

Direct memory access (DMA) is driven by the event when each of the individual buffer block is fully filled with the sample points. The rate of fetching event relies on the clock cycle operated by the FPGA time-base clock. The digital trigger begins the sample storing action. Then the direct memory access function waits until the buffer to be filled. When this event occurs a single

block of buffer memory gets transferred to PC memory space. The concurrent digitizing action and transferring action provides consecutive data stream of each echo with different phase encoding steps. In order to handle large data stream generated by multiple A/D convertor in different input channel, circular buffer needs to be implemented. Circular buffer structure provides transferring mechanism that reutilizes the memory space which has been used to capture previous signals. First, a circular buffer starts to fetch the data of determined length defined by single buffer block. When memory space is fully allocated with incoming data stream the mechanism starts overwriting the previous data sets at each subsequent triggered cycle. This process is driven by FIFO buffering action. This data structure provides a transferring mechanism that would continuously acquire data.

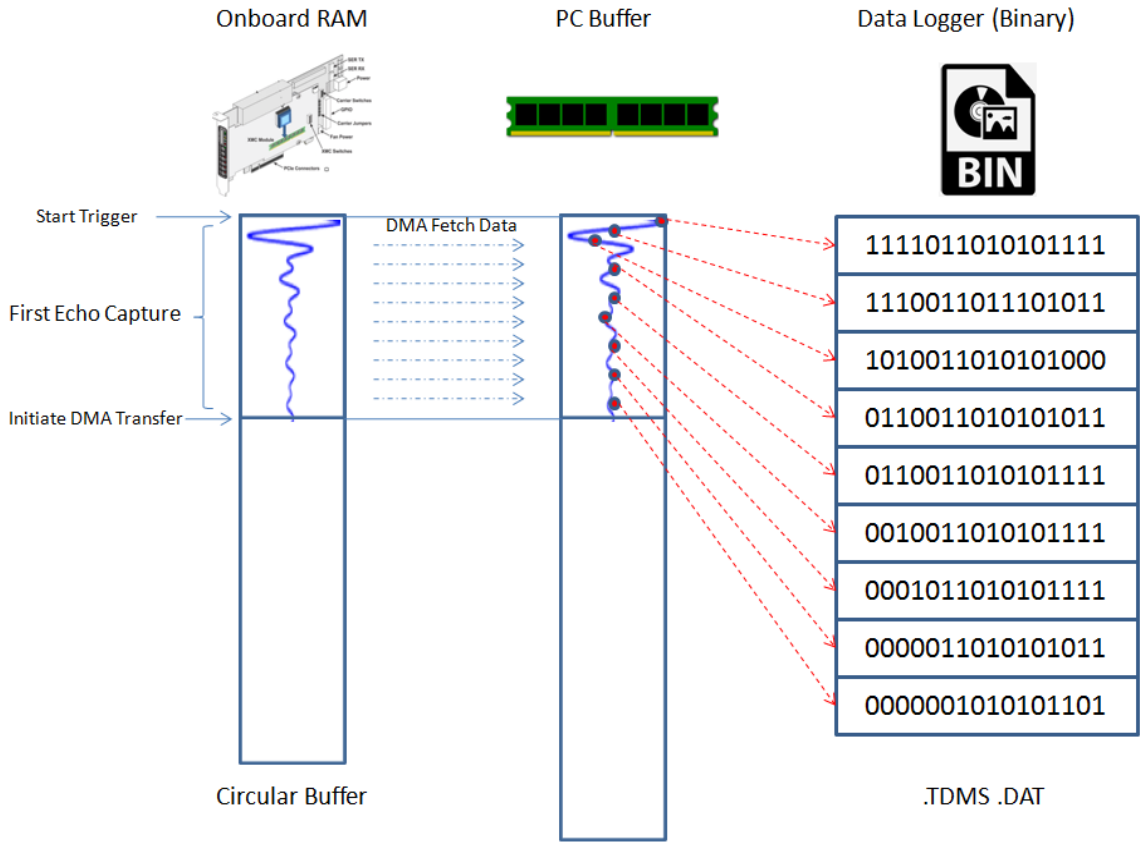


Figure 14 Streamed Data Transfer for first echo capture

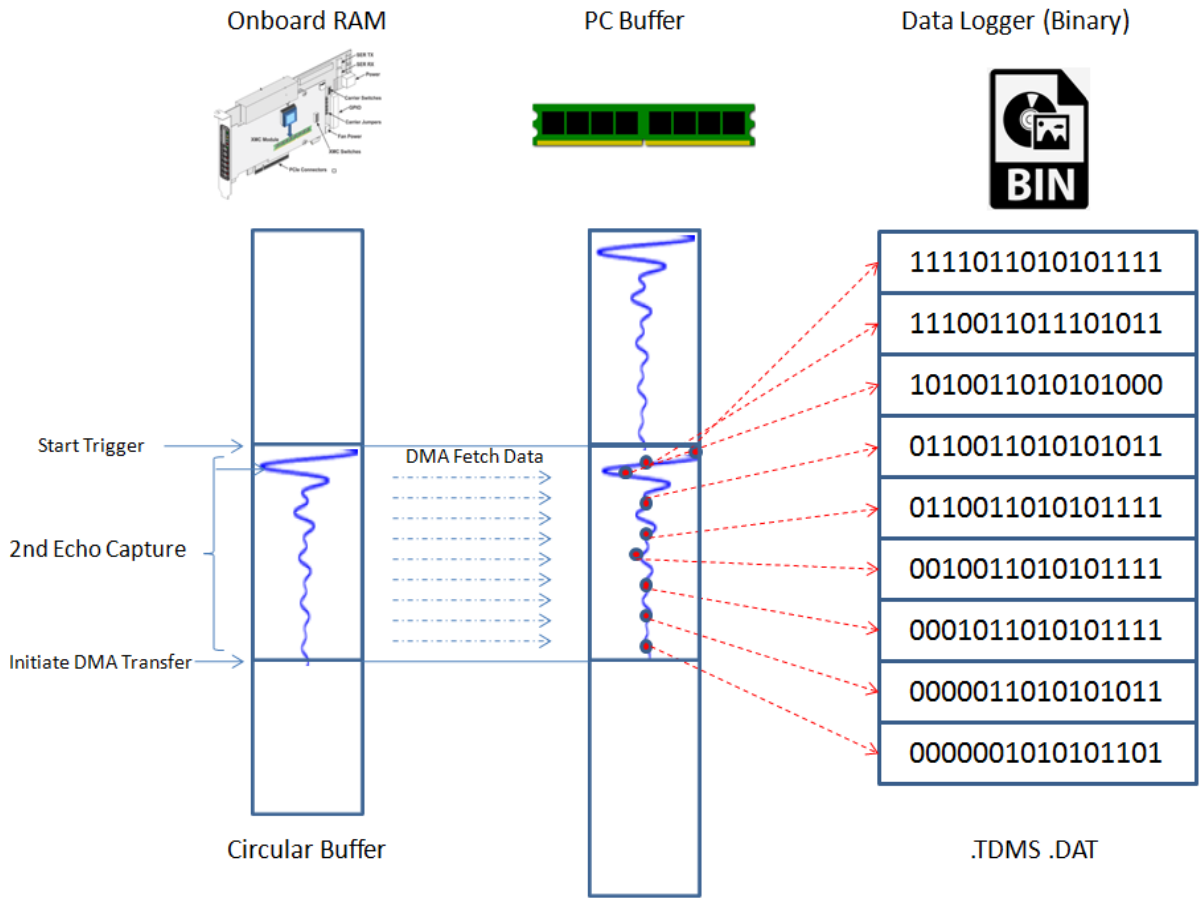


Figure 15 Streamed Data Transfer for second echo capture

Concurrent action of data filling and data emptying process executes its action at a different rate. While FIFO buffer continues to write data, the direct memory access (DMA) keeps on emptying the on-board memory space. To achieve continuous data flow DMA is required to fetch the data from the buffer fast enough rate to prevent the remaining data from being overwritten by the incoming data. Speedy time-base clock of FPGA assures the data to be fetched at high rate. PCI-express bus utilizes multiple lanes in the data handling bus (e.g. x4, x8, x16). To guarantee data emptying process is faster than the data filling rate, double buffering algorithm can be utilized in parallel data transferring process..

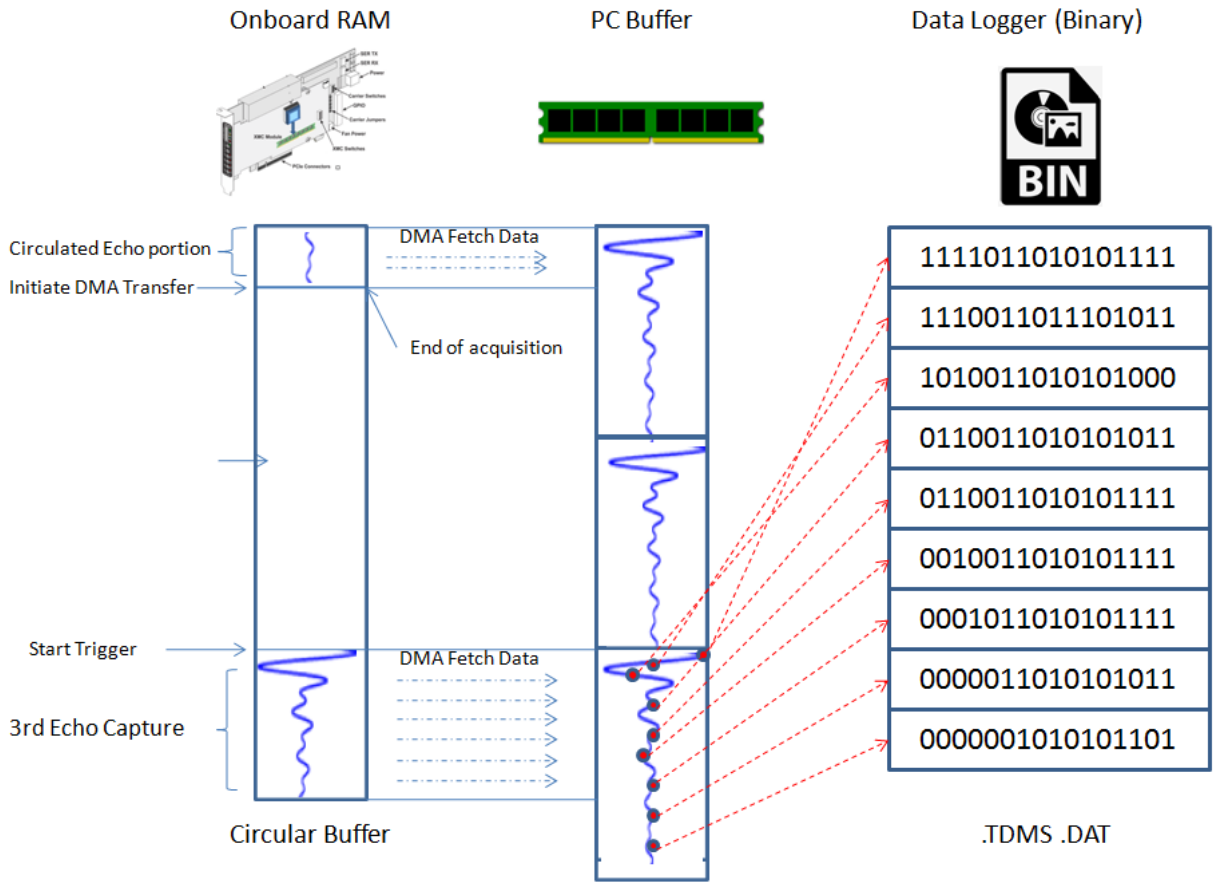


Figure 16 Circulated buffer stream for third echo capture

Direct memory access fetches data at a rate that corresponds to the FPGA time base clock . The DMA fetched buffer size ranges from 1 byte to 1000 byte. The FPGA time base clock that sets the recursive data transferring process, normally ranges from 10MHz to 80MHz for Xilinx Kintex FPGA chip. This fully supports the maximum input rate of 200MHz for the ADC. This provides enough memory space on onboard memory to prevent previous data from being overwritten by the newly acquired data. When onboard memory reaches its maximum capacity, circular buffer allows to continuously store data by circulating the data stream from the beginning.

3.4 Digital Down Conversion

The Digital Down Conversion logic is implemented in Xilinx Kintex FPGA chip for Pentek 78862. The wide range of reconfigurable logic gates within FPGA provides strong adaptability with high-speed and improved accuracy in digital signal processing. In NMR application, implementation of digital down conversion is essential because the system deals with high frequency RF signals. When NMR signal lies in higher the frequency band, the receiver needs to digitize sample in much faster rate. This circumstance generates large input data stream in the buffer to suffice Nyquist frequency with high digitization rate. Reduction of data is required as the system gets to deal with signal composed of higher frequency. Developing software based DDC architecture in digital domain has great advantages over analog hardware based architecture. Discrete nature of digital data provides implemented logics to be more stable over the analog components. Operating signal processing in digital domain facilitates the signal capture in baseband.

DSP Logic blocks deployed in FPGA provides improved component lenience over analog components to operate signal processing in much precise fashion. Every components in the DDC core are constructed in aspect of software to capture high frequency FID signal in NMR applications. Software define radio components in DDC core provides great adjustability when it comes to controlling the center frequency and bandwidth of the band-pass filter. Wide range of decimation factors can be applied in digital decimator to omit sample points to decrease the amount of data to be processed. The FPGA DDC core consist of three main subcomponents: frequency tuner (local oscillator), band-pass filter (BPF), low-pass filter (LPF) and a sample

decimator. Frequency tuner (oscillator) is used to change the frequency of an RF signal into a intermediated frequency (IF) band while preserving all other characteristics of the acquired RF signals regarding to phase and amplitude. Converting frequency in to lower intermediate frequency band allows the RF receiver to sample more data points in one period cycle of the RF signal. In order to prevent frequency distortion, at least two sample point are required to preserve the all frequency content during acquisition. The digital mixed down stage is configured through numerical controlled oscillator (NCO) to provide more sample point per period cycle.

Once the digital down conversion core translates the RF signal down to a intermediate frequency (IF), the undesired high frequency components and noise that exists close to baseband can be filtered with the low-pass filter. The DDC core filter admits all signal that consist frequency within Nyquist frequency passband. Decimation factor and sample frequency defined by Nyquist frequency sets the intermediate signal bandwidth of the receiver. DDC core filters are design to take software parameters from APIs to programmatically control the spectrum region of interest. This allows the device to captures frequencies below its cutoff frequency and rejects all other signals. The cutoff frequency is simply controlled by the decimation factor and sampling rate. NMR RF receiver are often dependent on multiple frequency on relationship to multiple nucleus. If the nucleus precession frequency reside above the Nyquist frequency in spectrum domain, the device can utilize the frequency tunable narrow band filter to tune the pass band for the aliased frequency. Signal that resides above Nyquist frequency generates the fold down image into the lower band. Aliased frequency is dependent on the sampling rate, f_s. The DDC core in Pentek 78862 defines the pass band to be 80% of the sampling frequency. Bandwidth of the FIR filter can be contracted with sample decimator to reduce the bandwidth. This neglects undesired signal

in the spectrum. The aliased signal lies under the fold back spectrum region while preserving phase and amplitude of the RF signal. For Pentek 78862, receiver bandwidth is configured by setting decimation factor N and the sampling rate of the A/D convertor. The receiver bandwidth utilizes 80% of the decimated sample frequency $f_{d.}$ The decimated sample frequency $f_{d.}$ uses the rate proportional to the decimation factor N. The relationship between sampling rate and receiver bandwidth is describe by the following equation

$$(f_d = (f_s / 2) / N)$$

DDC FIR filter component is design to provide 3db pass band at 80% of the spectral region covered by the Nyquist frequency. The result of signal capture referenced from the baseband is represented with the following relationship utilizing 80% passband characteristic of the low pass filter.

$$f_d = (0.8 * (f_s / 2)) / N$$

3.5 Synchronization and Phase Locked Loop

Phase Locked Loop(PLL) is a technique commonly used on RF transceivers to synchronize sample clocks with a accurate reference source. This instrumentation technique essentially provides feedback control loop to compensate for phase shift cause by jitter. While a PLL is used in variety of RF transceiver system, it is also sufficient to implement this in software define radio DDC core to adjust the phase and frequency of the input signal in digital domain. The PLL control feedback loop provides an algorithm to fine-tune the numerical control oscillator as a

compensator by deriving phase error from the phase detector so that the eventual phase error decrease with certain contraction ratio. A phase locked loop compares the phase of a reference signal. The phase reference is generally provide by voltage-controlled crystal oscillator (VCXO) in its control loop to the phase of an configurable feedback signal. When the phase comparison contracts to compute phase difference between the sample clock and the synchronization clock to be zero in the negative feedback control loop, the control loop reaches its equilibrium to have exact phase match between the sampling clock and reference clock.

PLL control loop consist of phase detector, loop filter, and the voltage-controlled crystal oscillator. The VCXO generates a accurate periodic reference signal and the phase detector evaluates the phase with the periodic input clock source compensating the phase difference to align the input clock source against the reference clock source. When acquiring signals in multiple channel, the sample clock derived at each channel experiences different phase due to jitter and triggering point. The phase difference between each channel can causes major problems in image reconstruction process, since perfect alignment of free induction decay signal needs to be accomplished in Fast Fourier Transform (FFT) process to avoid images artifacts. Phase correction in image processing could be rather difficult in post processing, since it is convoluted to analyze the phase shift of the Free Induction Decay signal between each echo without any start reference point in the acquired data. Implementation of the PLL control feedback provides synchronization mechanism to prevent phase jitter from happening. Also phase alignment of PLL feedback loop allows the device to synchronize multiple channel with a single reference clock source generated by voltage-controlled crystal oscillator (VCXO).

3.6 Nyquist Frequency and Aliasing

When the RF receiver acquires free induction decay (FID) signal, the samples are digitized into a sequence of discrete data. The discrete sample points are stored in memory with a speed define by the sample clock. The concept of analog signal lies with the aspect that the infinite amount of sample are accrued to represent continuous waveform. Once analog signal is converted to digital domain, sequence of finite analog sample points are represented in discrete fashion. Pentek 78862, RF receiver sample discrete samples supporting rate up to 200MS/second. Different nucleus or particle has its own resonance frequency due to various of gyromagnetic ratio (γ) in NMR signal acquisition. Under the identically applied filed $B_{0,}$ each nuclei experience unique spin or angular momentum to have specific precession frequency, f_0. Larmor's equation best describes this precession frequency as the following.

$$f_0. = \gamma * B_0$$

Precession Frequency	$= f_0$
Gyromagnetic ratio	$= \gamma$ (MHz/ Tesla)
Applied field strength	$= B_0$ (Tesla)

In a field (B_0) of 4.7 Tesla, the resonance frequency of ^{2}H, ^{23}NA, ^{1}H is computed to be

200.112MHz = (42.577 MHz/T) * (4.7 Tesla),

52.931MHz = (11.262 MHz/T) * (4.7 Tesla),

30.719MHz = (6.536 MHz/T) * (4.7 Tesla),

respectively due to its own unique precession frequency. To capture its precession rate and to represent its frequency component in a correct fashion, the samples needs to be taken at a specific sampling rate. If the device doesn't sample the data in a sufficient amount speed the

captured discrete sample would represent frequency component in a different spectrum region and this distorted frequency representation is known as an aliasing.

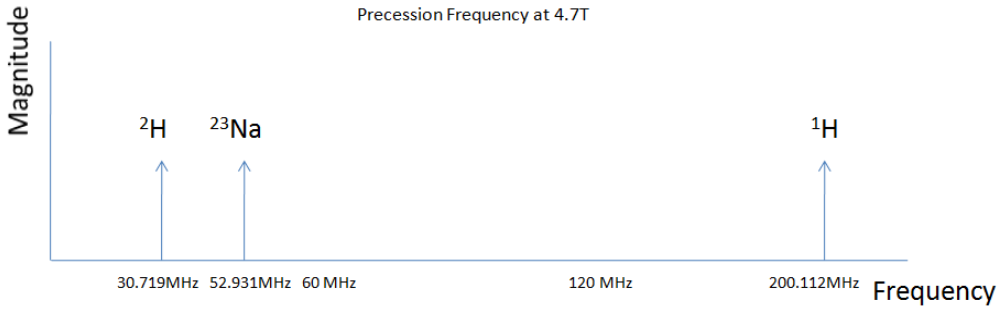


Figure 17 ^{2}H, ^{23}NA, ^{1}H Precession frequency spectrum at 4.7T

With the sampling rate of 120MHz, Nyquist frequency is set to be 60MHz, due to the fact that at least two samples are required in each period to preserve the frequency. In a field (B_0) of 4.7 Tesla, the precession rate of ^{2}H, and ^{23}Na lies under the Nyquist frequency in the spectrum, and ^{1}H is placed above the Nyquist frequency. These signals from ^{2}H and ^{23}NA remains to stay at the same region of spectrum since it suffices the Nyquist frequency ^{1}H signal gets fold down to a frequency of 39.88 MHz with sampling rate set to 120MHz.

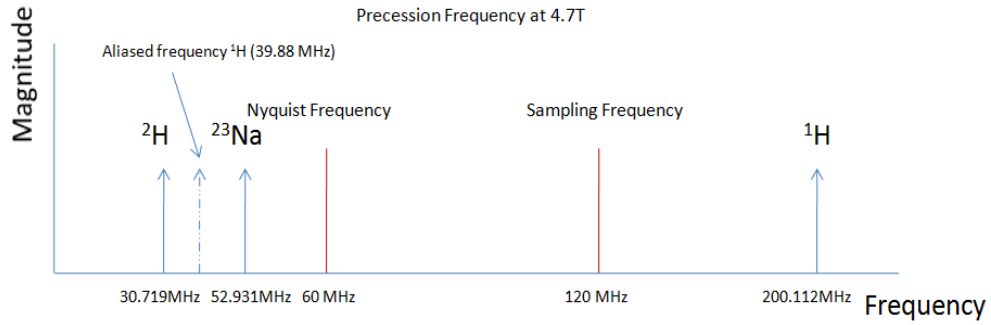


Figure 18 ^{1}H aliased frequency with 120MHz sample rate

When a signal is not sufficiently sampled at fast enough rate, aliasing phenomenon can occur. Sampling rate that doesn't suffice 2 times of the maximum frequency, would mistranslate the true nuclei precession frequency. It is important to note that aliased signal capture does not misrepresent the amplitude and phase of the FID signal for each nuclei. This implies that capturing aliased signal of certain nucleus would let system to preserve all necessary information regarding to the signal. Since translated aliased frequency has unique relationship between the sampling rate and the resonance frequency, the system can restore its true precession rate as long as the aliased frequency does not overlap with other nucleus precession frequency in spectrum.

3.7 Wideband RF signal acquisition

Wideband RF receiver relies on the direct sampling technique. This signal acquisition method relies on the A/D convertor performance to capture the signal lying under the Nyquist frequency in the spectrum. The architecture consist A/D convertor followed by software define FIR filter in FPGA. The wideband RF receiver operating in broadband mode does not have any mixed down stages and the hardware presence of the local oscillator is not required. Operating NMR signal acquisition in wideband mode in the receiver, transfers every discrete sample to the memory space when no decimation factor is configured in the DDC core. The system can utilize the digital down conversion (DDC) core in FPGA instead of using a mixer to isolate signal. The maximum bandwidth achieved in direct RF sampling mode is defined by the sampling rate and decimator function implemented in DDC core. Anti-aliasing filter would not be implemented neither prior to the ADC, nor in the DDC core. This would even capture nucleus precession frequency existing above the Nyquist frequency in the spectra. In the case where the decimator

function is enable in the DDC core, the allowable maximum bandwidth contracts accordingly to the decimation ration. The bandwidth in this case develop into a function of sampling rate and the decimation ratio as the following

$$f_d = (0.8 * f_{Nyquist}) / \text{ Decimation factor}$$

The acquirable frequency region in the spectrum is purely defined by the FIR filter bandwidth and numerically controlled oscillator (NCO) in FPGA. Software logic reallocates the center frequency of the pass band by tuning the digital numerical oscillator frequency. When sampling rate is set at 120MHz, the Nyquist Frequency becomes half of define sampling rate (60MHz).

$$f_{Nyquist} = f_s / 2$$
$$60\text{MHz} = 120\text{MHz} / 2$$

Decimation factor of 2 provides acquisition bandwidth of 24MHz. Numerical control oscillator (NCO) in DDC can set the center frequency of the FIR filter from 0 ~ 60 MHz due to band tune the region of interest in the spectrum.

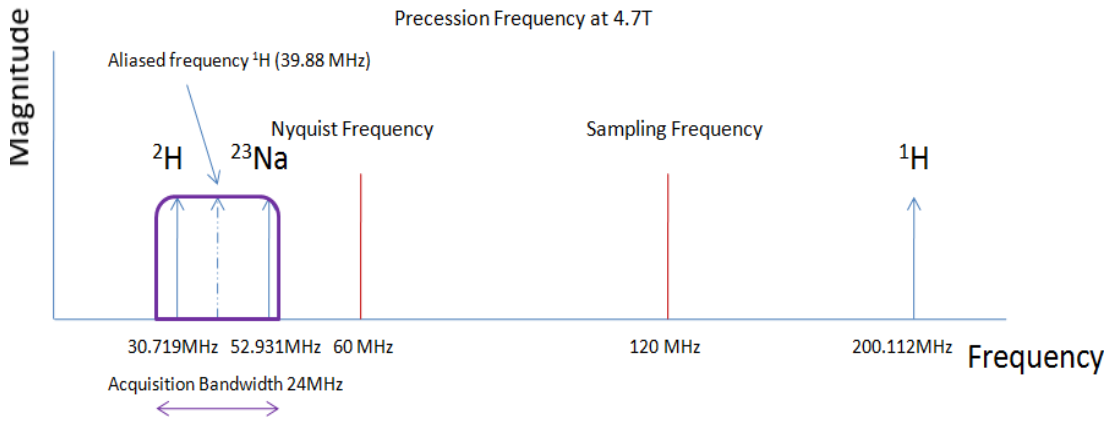


Figure 19 Wideband acquisition 120MHz sample rate and decimation ratio of 2

3.8 Narrowband RF signal acquisition

Pentek DDC core is able to perform digital down conversion (DDC) and the IP core executes its decimator to contract the enabled wideband signal down to a smaller bandwidth by extracting samples that are only needed for capturing the frequency component. Software defined radio (SDR) provides a way to operate signal acquisition in wideband or narrowband. The purpose of using narrowband acquisition mode in device is to extract specific frequency band to reduce the amount of data samples. One of the drawback in wideband acquisition mode is that undesired noise signals are captured along with the resonance frequency of multiple nucleuses. The noise existing in wide range of frequency degrades the performance in signal to noise ratio. Also captured signal with large acquisition bandwidth produces more data.This generates more processing load on the data transferring bus and direct memory access (DMA).

The bandwidth in narrow band sub-channel mode is defined by sampling rate and the decimation ratio. The bandwidth in narrowband acquisition mode is computed in same way as the wideband acquisition mode. The difference is the 8 independent sub-channel DDC core can be simultaneously applied for single acquisition channel. The FIR filter for each DDC core can be tuned to a specific region with offset to capture desire signal. For applications where the sampling rate set at 120MHz, the Nyquist Frequency exist at 60MHz. Acquisition bandwidth for each sub-channel can be represented as the following

$$f_d = (0.8 * f_{Nyquist}) / \text{ Decimation factor}$$

$$f_d = (0.8 * 60\text{MHz}) / \text{ Decimation factor}$$

$$f_d = (48\ \text{MHz}) / \text{ Decimation factor}$$

Decimation factor of 6 provides acquisition bandwidth of 8MHz. Numerical control oscillator in DDC can set the center frequency of the FIR filter from 0 ~ 60 MHz. Parallel DDC core can be simultaneously allocate different frequency band with frequency offset defined in software to differentiate the channel band.

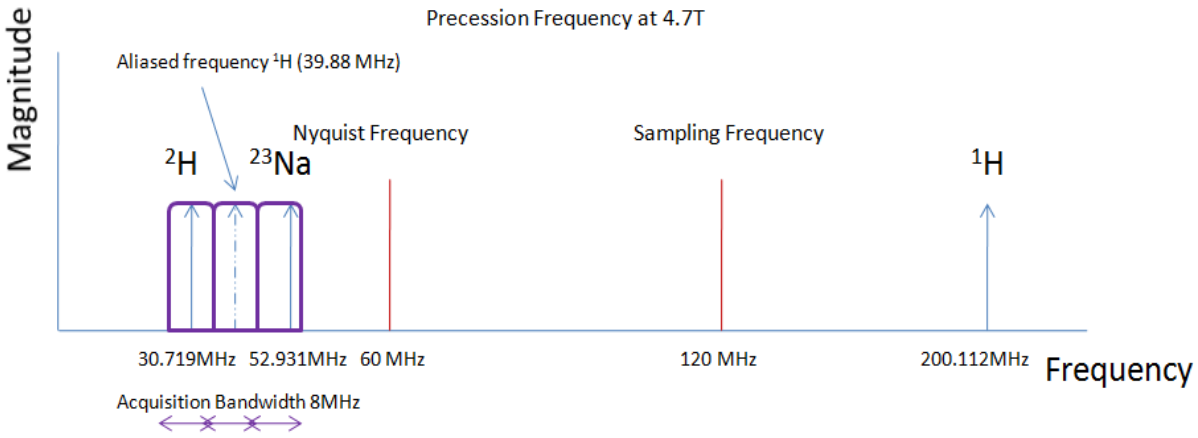


Figure 20 Narrowband acquisition with 120MHz sample rate & decimation ratio of 6

Narrow band acquisition mode can expand its band selection capability by implementing parallel DDC core running independently to extract specific signals from a designated FIR filter in the software. Operating multiple DDC core allows the system to implement band tunable sub-channels. This software architecture allows the system to assign specific frequency band for each sub-channel. The narrowband acquisition mode is optimized method to reduce the amount of being captured. The narrowband mode allows the system to only extract desired nucleus resonance frequency component. The band tunable filter allows the system to neglect all unwanted noise or aliased signals from be captured by the system.

4. DEVICE CONTROL SOFTWARE OVERVIEW

4.1 Acquisition Configuration Parameters

The DDC core implemented in Pentek 78862 FPGA provides two distinctive acquisition mode, single-channel wideband signal capture mode, and the multi-band tunable 8-channel mode. Pentek Navigator™ Board Support Package (BSP) provides device drivers and application programming interface (API) to provide complete control of wideband and multiband NMR signal capture. The API consist of specific command interfaces to control the receiver and it includes general command routines to access the DDC core logic implemented in FPGA.

In this research, majority RF acquisition software are developed with a degree of flexibility to accommodate different set-up of NMR experiments. The acquisition engine performance can be altered by providing different command parameters dynamically. The acquisition control is first achieved by sending the configuration arguments to provide initial setting for the device. Based on this settings then the runtime engine executes device initialization, re-arming of the trigger and digitization of the data. Runtime engine takes command arguments dynamically during the acquisition to monitor and handle error state in data transferring stage. The general control scheme is to first send command argument to configure ADC related setting and FPGA IP core parameters to run customized NMR experiments. In runtime, hardware component initiates all of its execution referring to the command arguments passes from the host user interface. All hardware related faults are monitored in runtime to make decision based on the current state of the engine execution status.

Different types of settings are configured statically, prior to the initiating the RF receivers . Following is the statically controlled arguments for Pentek 78862 in Navigator™ Board Support Package (BSP).

Board Clock Source - The argument needs to configure to set whether the device would select internal voltage controlled oscillator (VCXO) or external clock as a synthesizer. This clock source is derive to provide digital pulse train for the sampling clock.

Board Clock Frequency - The Synthesizer clock rate need to be configure prior to initiating the acquisition The maximum rate of the broad clock is 250MHz. Different clock rate can synthesize through integer division. This parameter sets the frequency of internal oscillator when clock source is set to the internal VCXO. When external board clock is supplied the frequency needs to be match using floating point representation.

Reference Clock Frequency - External reference clock could be supplied to provide phase locked loop control. This provides phase stability of the sampling clock in the ADC and prevents phase jitter to be compensated through clock synchronization. Configuration of reference clock is optional and the floating point argument needs to match the speed of the frequency of the externally supplied clock

Channel - This argument specifies the acquisition channel source. it can be configured to specify multiple channels or single channel. The device can be configured to utilizes single, dual, triple, or quad channels in any combination.

Data Packing Mode - This parameter defines the binary packing format of the AD convertor. For real data, the runtime engine stores consecutive 16 bit binary data in to a 32 bit word format. When acquisition mode is set to collect IQ data, the arguments needs to be configure to either store consecutive 16 bit IQ data into 32 bit word format or two consecutive 24 bit IQ data into a 32 bit word format. When 24 bit IQ data is stored in two 32 bit word data type, unused 8 bit data will be filled with 0.

ADC Sample Rate - This argument represent the ADC sample clock speed. It uses the floating point format and the value must be a factor of board clock frequency. The dividing factor must be 1, 2, 4, 8, or 16. Each acquisition channel has dedicated ADCs and independent clock rate can be set to digitize sample at different rate.

ADC Trigger Source - This parameter need to specify whether the digital start trigger would take its TTL source from the internal registry or front panel SMC trigger input. Trigger source can be disable to neglect trigger based acquisition mode.

ADC Synchronization Source - This parameter need to specify whether the synchronization clock would take its TTL source from the internal registry or front panel Sync/Gate input. This parameter is used when multiple board is being utilized to synchronize the sample clock and the trigger. The board serving as the Master must provide reference signal source to a Slave device. All Slave devices needs to specify the signal source to provide the same reference between the devices

ADC Trigger Polarity - This argument needs to be specified to define whether the ADC would start acquiring base on the digital rising edge or digital falling edge of the TTL source.

ADC Sync Polarity - This argument needs to be specified to define whether the ADC would synchronize shared clock and reference signal base on the digital rising edge or digital falling edge of the TTL source.

DDC Gain - The argument represent the DDC gain in integer value. The DDC core integrates software define amplifiers. Amplifier gain can be altered by this parameter setting.

DDC Decimation - The DDC core is integrated with the sample decimator to omit sample point by this factor. Each independent DDC core can set different value of decimation ratio ranging from 1 to 32. When multiple sub-channels are configure in narrowband acquisition mode the common decimation factor is applied to all sub-channel.

DDC Tuning Frequency - This argument specifies the center frequency of FIR filter band. When When multiple sub-channels are configure in narrowband acquisition mode the each sub channel can configure its own unique tuning frequency to select the band of interest. This parameter assigns the floating point representation into a numerically controlled oscillator (NCO) to adjust the signal capture band in the spectrum.

Data file format - This argument selects the data file format to be written to a file in the data logging process engine in run time. The command parameter can either select file format in

binary or asci. The binary file consist data in raw binary representation and it has a file extension of (.dat). The asci file format consist data in signed integer representation ranging its value from -32768 to 32767. The asci file format will have name with a (.txt) extension.

Data Fetch size - This argument represent the data size to be written to a file for each triggered block. For NMR acquisition This would represent the data size of the single echo capture.

Number of buffer blocks - This argument represents the number of buffer blocks employed in the onboard memory. This parameter needs to be set the number of direct memory access (DMA) buffers of each data fetching cycle. The individual buffer blocks are utilized to create circular buffer to support continuous time acquisition.

Size of the buffer - This argument needs to set in run-time engine to implicate the transfer size in number of bytes. The parameter indicate the total transfer size of the single buffer block. Direct memory access (DMA) function fetches an amount of the data configured by this argument at each recursive iteration cycle.

Board Reference - This argument represents the device index value in case when multiple boards are used for acquisition. To identify the device resources between multiple boards this reference index will be used to distinguish dedicated command routines for each devices.

Acquisition Loop - This argument need to configure in Navigator BSP acquisition engine to implicate the number of acquisition cycle. For trigger based acquisition the number of

acquisition loops need to represent the number of trigger blocks. In NMR signal acquisition it is typical to set 64, 128, 256, or 512 to match the number of phase encoding steps to run consecutive echo capture.

4.2 Application Programming Interface

Navigator™ Board Support Package (BSP) provides application programming interface to access functions regarding to ADC, DDC, Trigger, DMA and Clock. Application Programming Interface (API) supports board level function in C++. Dynamic Link Library can be imported to LabVIEW to generate execution function in virtual instrument (VI) format. The following is the list of core APIs to execute acquisition along with the FPGA IP cores. All command APIs are provided by Pentek BSP package and the following VIs are the direct translation of Pentek APIs.

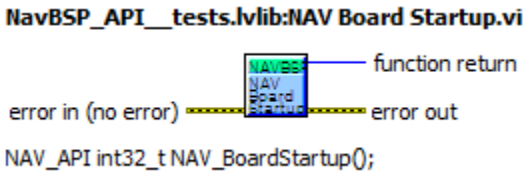


Figure 21 NAV Board Startup.vi

NAV Board Startup - This command initiates the device acquisition engine for the Navigator Board Library. This function initializes all hardware component within the device (e.g Clock resources, Trigger, Digital Down Conversion , DMA). The routine needs to be executed prior to configuring other function. The function return provides error status in integer format when the fault has occurred in the startup process.

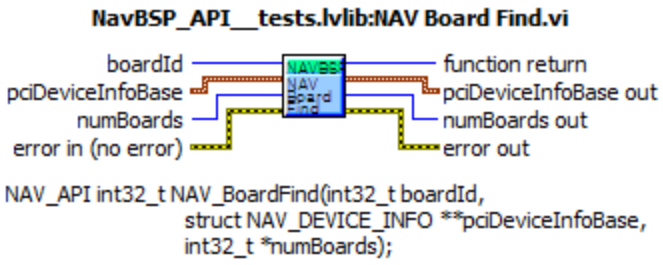


Figure 22 NAV Board Find.vi

NAV Board Find - This command searches for the device integrated in the system. It assigns board Identification reference number to a specific device to differentiate the boards. The function outputs an number of boards detected in the system as a integer value. The function return provides error status in integer format when the fault has occurred in the board detection process.

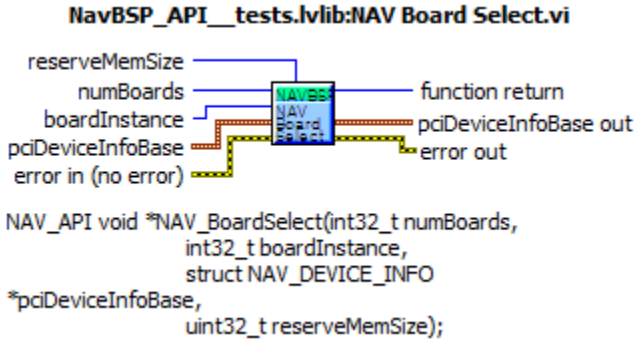


Figure 23 NAV Board Select.vi

NAV Board Select - This command selects the specified board by assigning board ID and returns the board reference as an output when multiple devices are being utilized in the system. The function return provides error status in integer when fault has occurred to provide board.

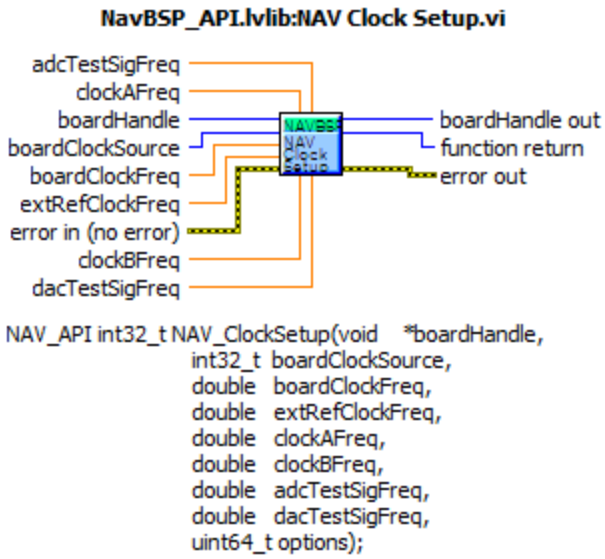


Figure 24 NAV Clock Setup.vi

NAV Clock Setup - This command configures all clock related properties within the device. Clock synthesis frequency , PLL synchronization clock frequency, sample clock rates are setup through the input parameter.

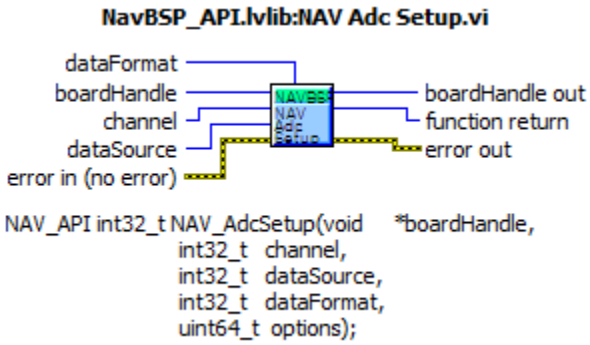


Figure 25 NAV ADC Setup.vi

NAV ADC Setup - This command sets up a ADC related properties. The channel can be specified with the data pack mode. The function selects the binary data pack mode. The function

stores real or IQ data in 32bit word formation The Board Handle parameter provides a reference to a specific board with pointer reference.

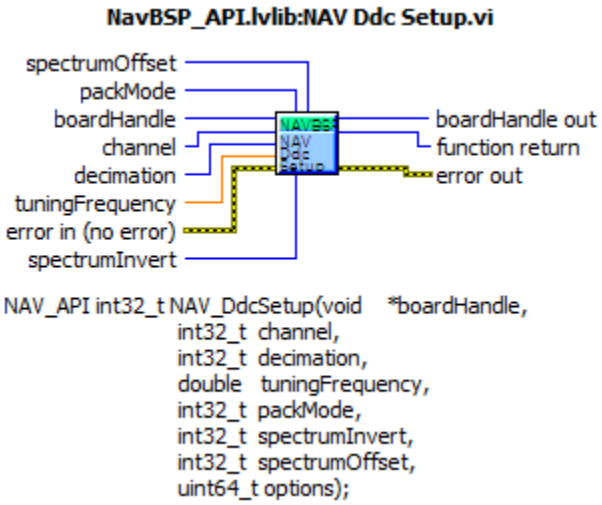


Figure 26 NAV DDC Setup.vi

NAV DDC Setup - This command configures the DDC core related parameters in FPGA. All arguments related to the filter, decimator, and local oscillator can be accessed with this function.

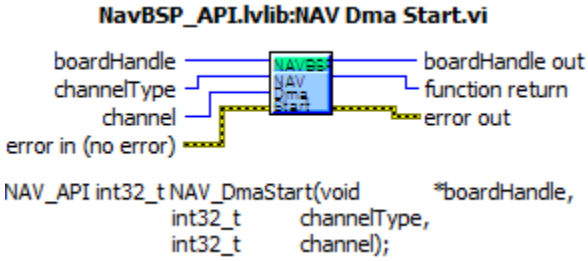


Figure 27 NAV DMA Start.vi

NAV DMA Start - This command initiates the DMA data transfer on a specified channel. It starts fetching data from onboard memory to a PC buffer.

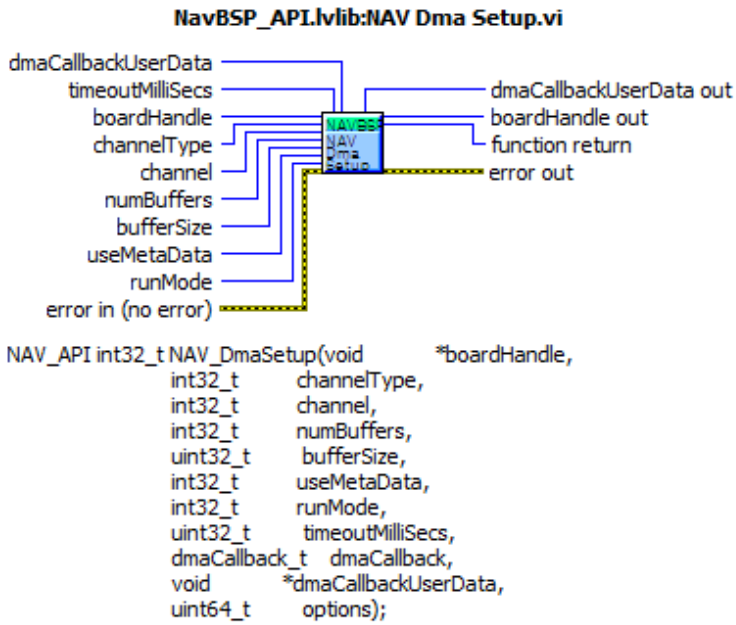


Figure 28 NAV DMA Setup

NAV DMA Setup - This command sets the single channel for DMA data transferring process. It provides access to the parameters like buffer size, number of buffer blocks, acquisition channel to construct a circular buffer in the onboard memory.

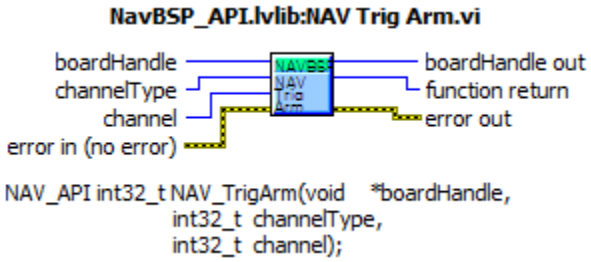


Figure 29 NAV Trig Arm

NAV Trig Arm - This command initiates the device to configure the digital TTL trigger for a specific channel. The start trigger would initiation the acquisition and store binary result with

the specified length of the buffer.

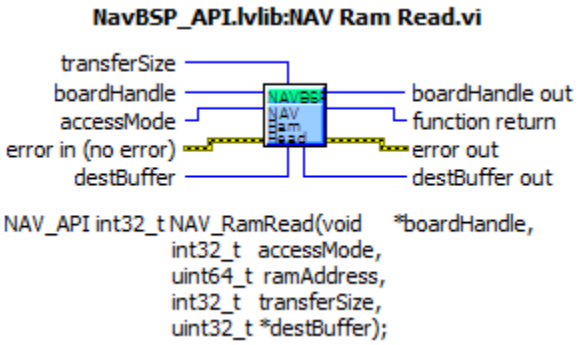


Figure 30 NAV RAM Read

NAV RAM Read - This Command initiates the data sampling process on a ADC and stores data in onboard memory.

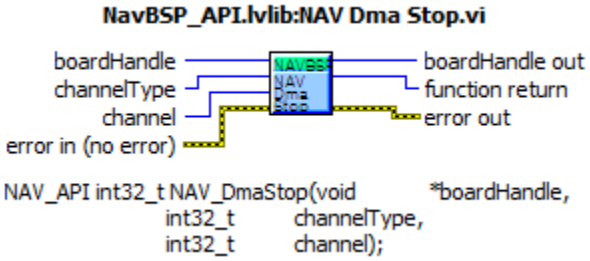


Figure 31 NAV Board Startup.vi

NAV Board Startup - This command terminates the DMA data transfer on a specified channel. The function monitors whether single buffer block is filled on onboard memory and terminates the data transfer to the PC buffer when single buffer is fully occupied with data stream.

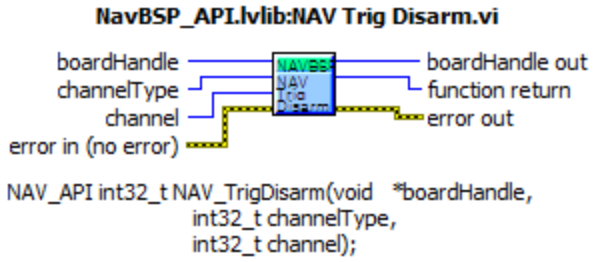


Figure 32 NAV Trig Disarm.vi

NAV Trig Disarm - This command disarms the trigger function. Front panel Trigger port would be deactivated to receive TTL signals.

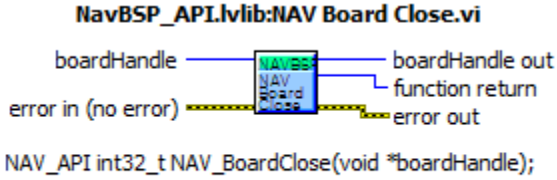


Figure 33 NAV Board Close.vi

NAV Board Close - This command terminates the board specific resources and releases all allocated memory space to close the acquisition engine in runtime.

4.3 Program Structure

Application programming Interface (API) needs to be structured in recursive command sequence to operate continuous triggered based RF signal capture. The transition between each command execution is driven by event status queried in the device. The decision process is required to

handle errors occurring in application runtime engine. For NMR continuous time acquisition, the instrument is required to first configure acquisition scenario with command argument provided by the API from the initial settings. Then the acquisition loop iteratively executes DMA buffer transfer and analog to digital conversion. Hardware interrupt process assure the instrument to be alarmed with any clock faults or device resource malfunction during the DMA process.

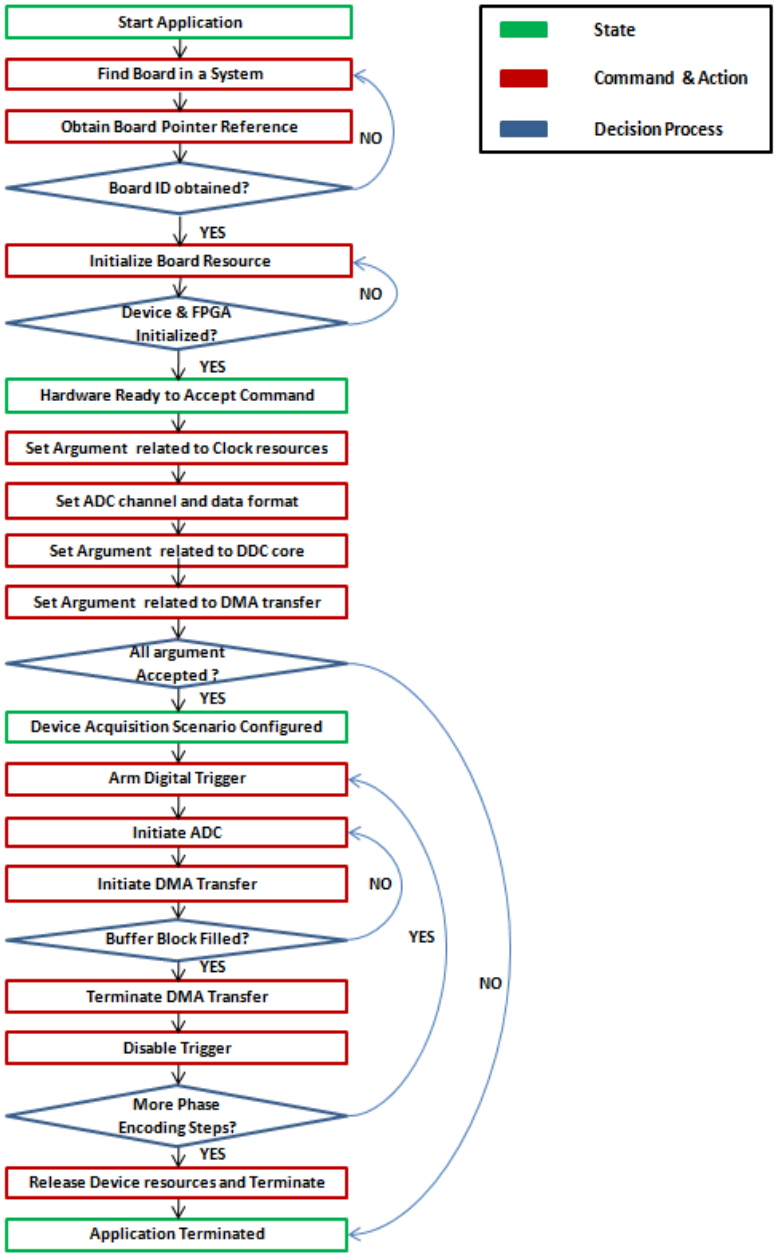


Figure 34 Acquisition state flow diagram in runtime engine

This algorithm provides a decision process between the acquisition steps to make transition to the following states to achieve API execution in sequential manner. In runtime, the control software monitors whether the device resources are executing the command properly. Once the acquisition is initiated the recursive data collecting sequence closely monitors the triggering and DMA data transfer.

4.4 Acquisition Engine

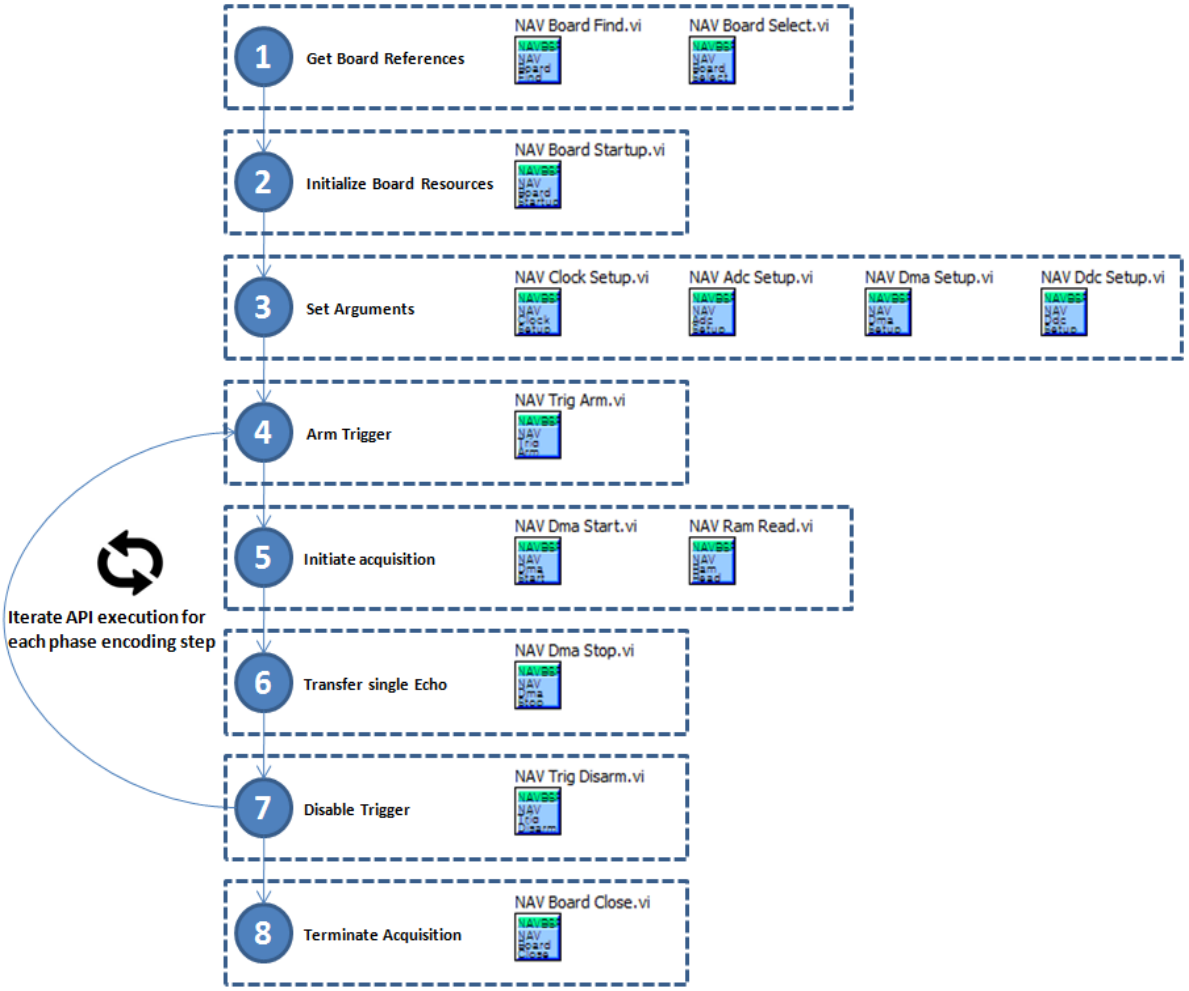


Figure 35 LabVIEW State Transition Layout

Board reference is obtained in a format of function pointers in LabVIEW. This board reference allows other API to set command arguments to the device. In order to implement the state flow of a recursive signal acquisition, at first the board resource get utilize with NAV Board Startup.VI and the arguments are configured with the setup VIs (e.g. NAV Clock Setup.vi, NAV ADC Setup.VI, NAV DMA Setup.VI and NAV DDC Setup.VI). For each phase encoding cycle NAV Trig Arm.VI and NAV Trig Disarm.VI would run repeatedly to reset digital start trigger. NAV DMA Start.VI initiates the data transfer and NAV RAM Read.VI fills discrete 16bit binary samples to the onboard memory. When the recursive process finishes acquiring all echo block, NAV Board Close.VI terminate the application and release all device related resource and sets all command arguments to a default setting.

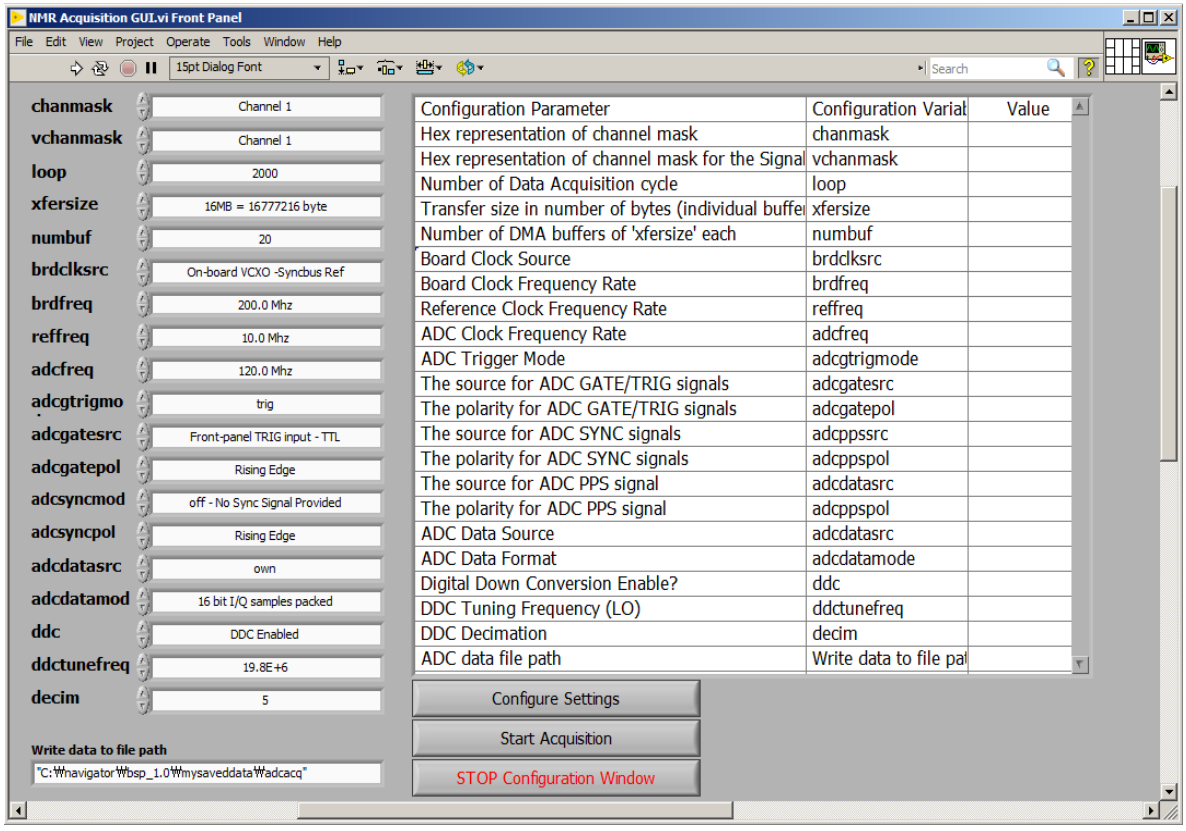


Figure 36 LabVIEW Graphical User Interface

4. 5 State Machine Design Pattern

State Machine Design pattern allows the software to execute sequence of command arguments dynamically. The RF receiver control logic has uniquely defined state which can lead the software to transit to one or more states. State transition can cover different types of scenario by querying hardware status through APIs in each command execution cycle. State Diagram graphically represents the different state existing in the control algorithm. In each state, the application executes different execution basing its decision on the outcome of the executed command. The transition between each state is accomplished by a unique decision process implemented in each state. The state transition logic can determine which state to make a transit to and predefined state transition logic handles this process at each case structure.

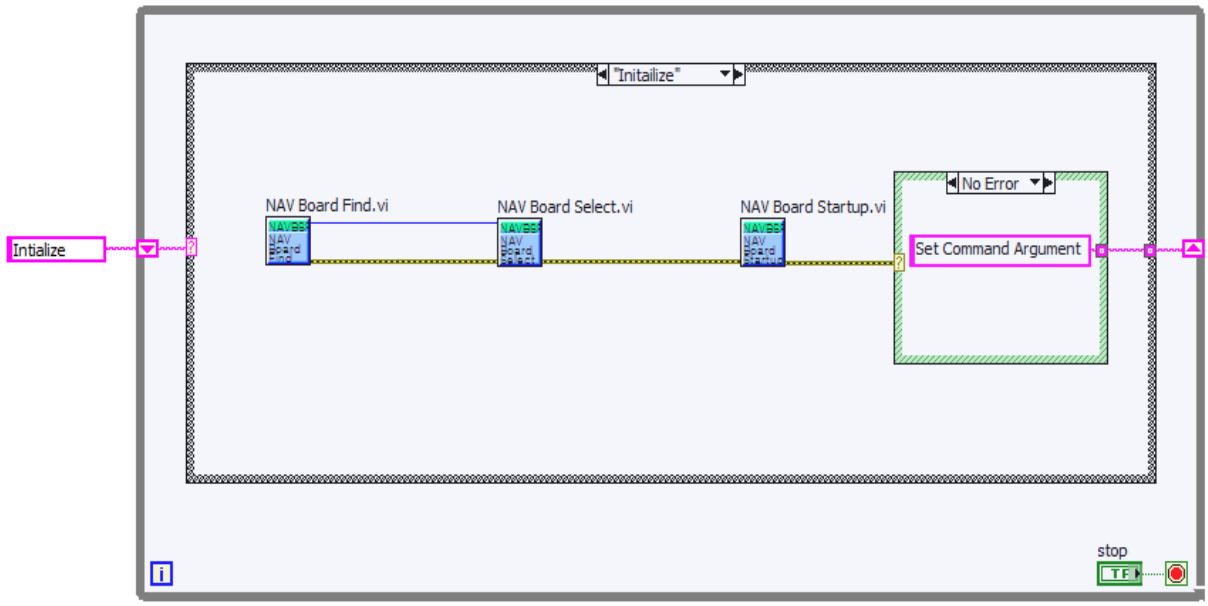


Figure 37 LabVIEW Board Initialize State

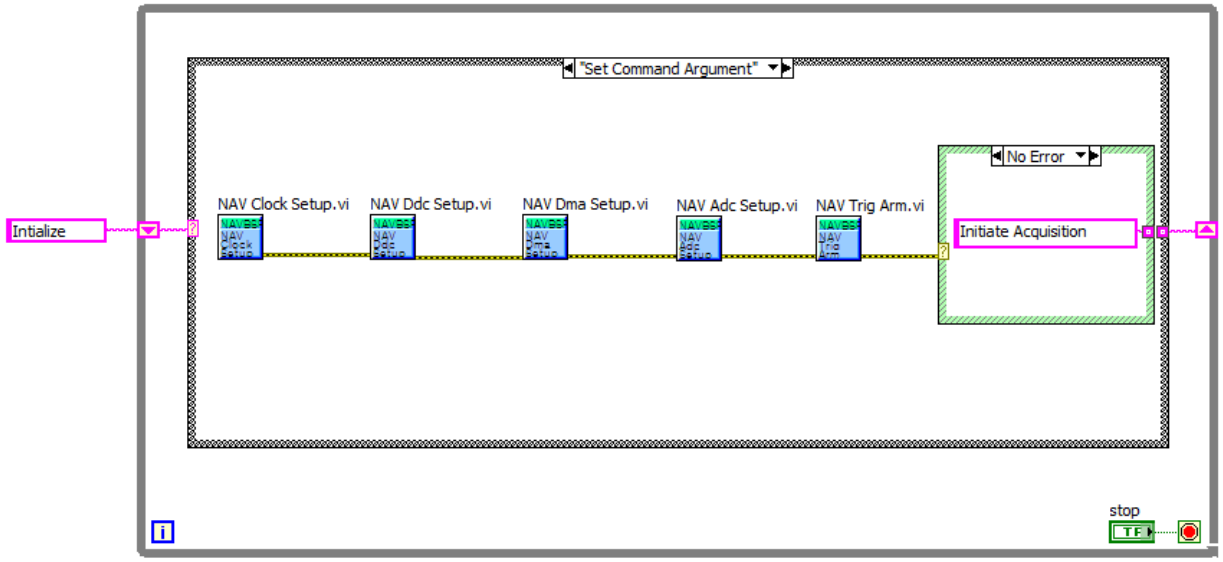


Figure 38 LabVIEW Set Argument State

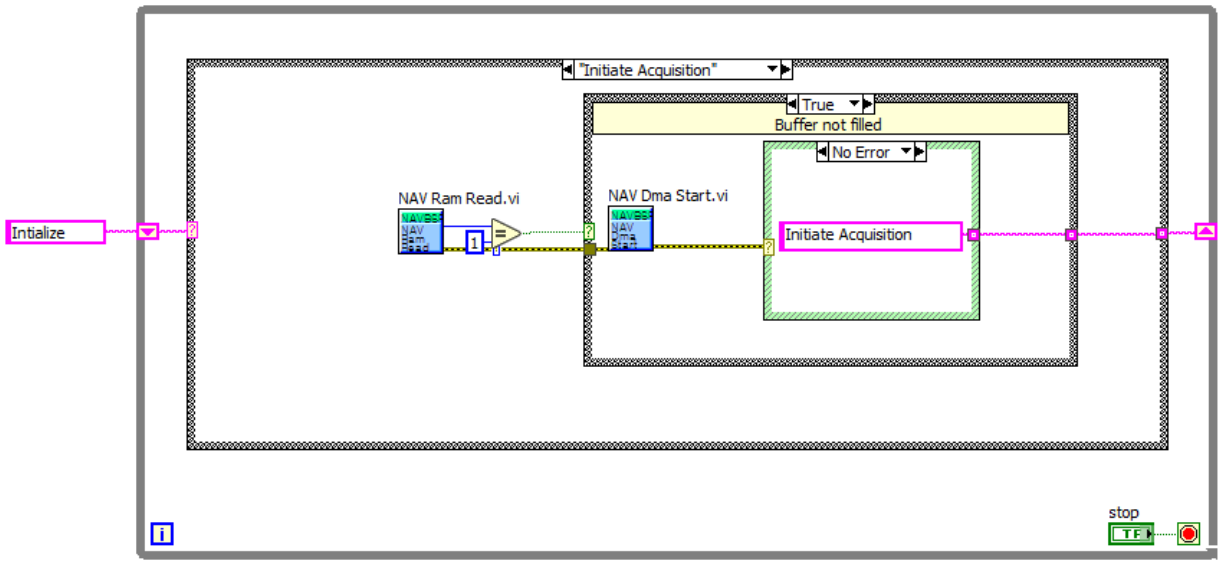


Figure 39 LabVIEW Initiate Acquisition & Start DMA Transfer State

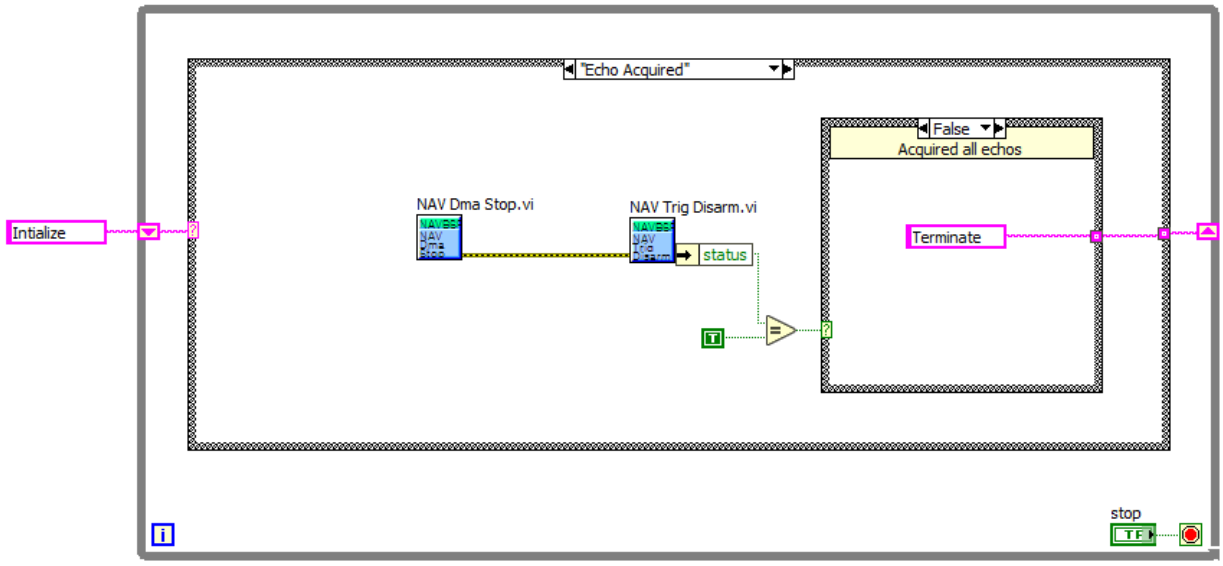


Figure 40 LabVIEW Echo Acquired & Stop DMA Transfer State

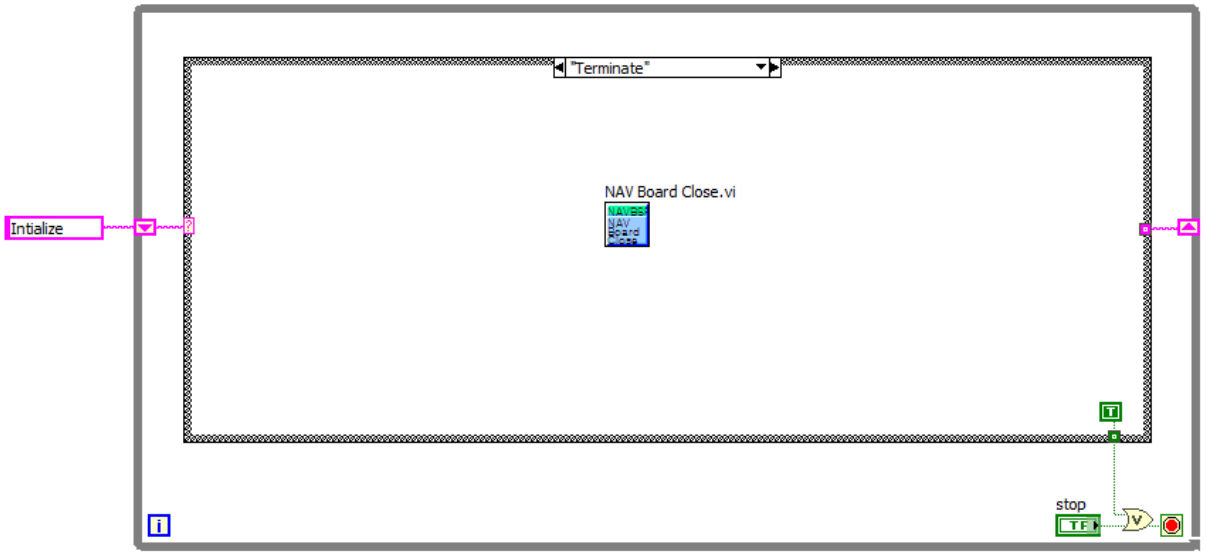


Figure 41 LabVIEW Terminate Application & Release Board Resources State

5. NMR ACQUISITION RESULTS

5.1 ^{1}H Magnetic Resonance Imaging

A matrix size of 512x128 image was constructed using Pentek 78862 narrowband acquisition mode. The processed image was compared with Varian acquired image at 4.7T, using a sphere-shaped phantom. 10.28ms long echo was captured utilizing 128 phase encoding steps with repetition time of 500ms. 1000us pulse duration was configured in a pulse sequence to generate RF Sinc signal for transmission. Pentek utilized 120MHz of sampling rate to capture its aliased ^{1}H precession frequency at 39.776MHz. The acquired image represents the slice thickness of 2mm of a sphere object. K-space was constructed based on the digital trigger to reference the starting point of each echo. 655.36ms of total echo was captured and referencing the digital trigger. Appended echo was parsed to form two dimensional K-space structure for image reconstruction.

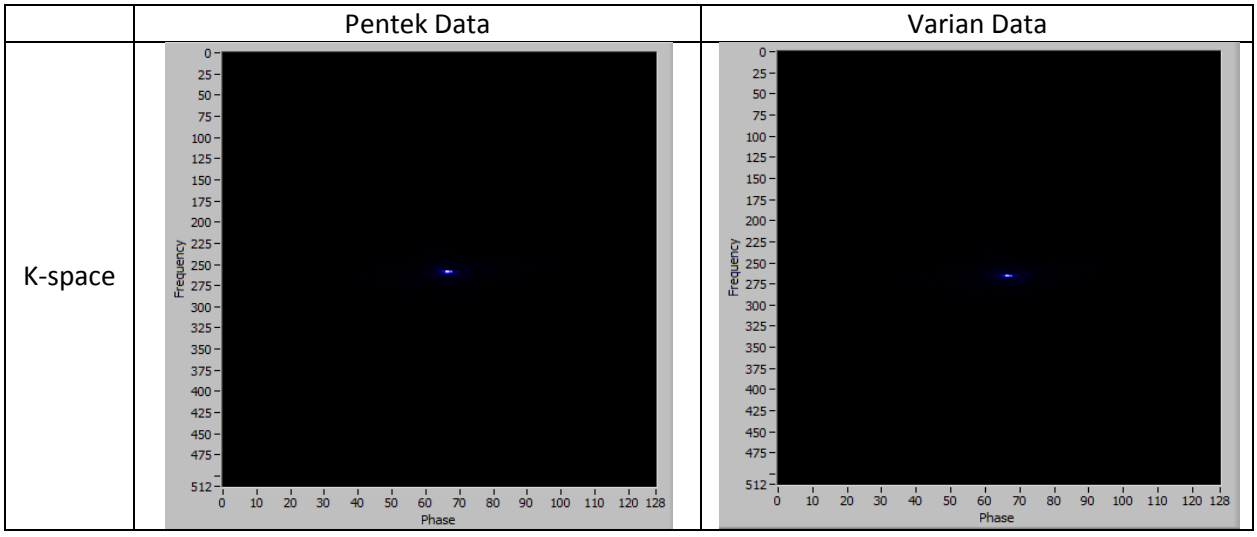


Figure 42 K-space of Pentek & Varian acquired echo (Phantom with ramp)

The image with the ramp pattern phantom was reconstructed using LabVIEW two-dimensional Inverse Fast Fourier Transformation (IFFT) function VI.

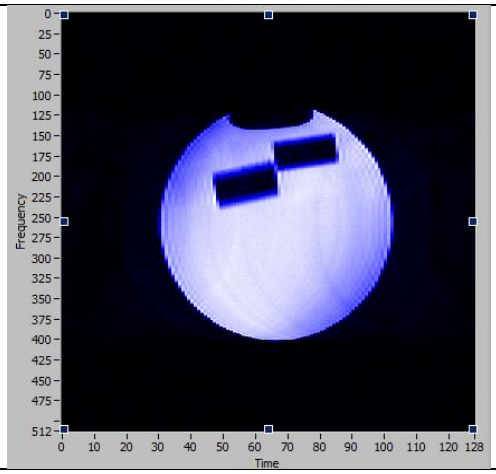
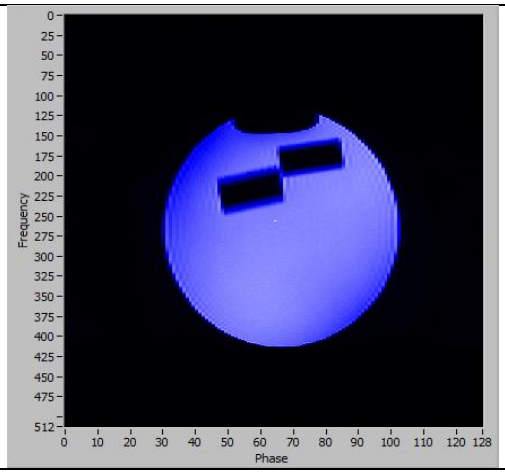
	Pentek Data	Varian Data
Image1		

Figure 43 Image Reconstruction with Pentek & Varian (Phantom with ramp)

The identical rectangular region was selected in the image to compute signal to noise ratio.

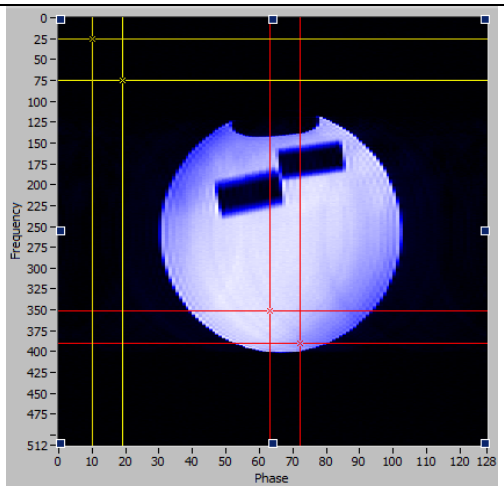
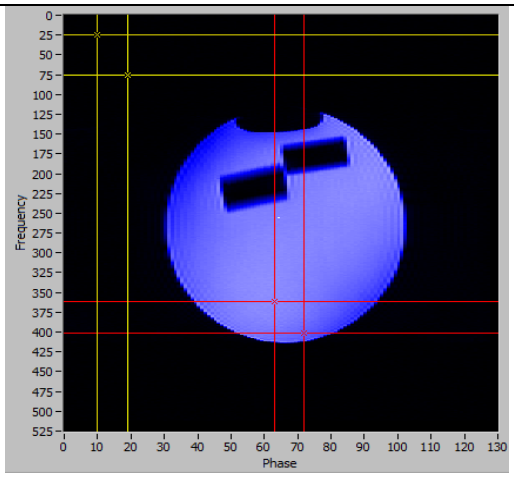
	Pentek Data	Varian Data
Image1	 SNR: 145.587	 SNR: 146.642

Figure 44 SNR comparison of Pentek & Varian (Phantom with ramp)

The image with the pin cushion pattern phantom was reconstructed using LabVIEW two-dimensional Inverse Fast Fourier Transformation (IFFT) function.

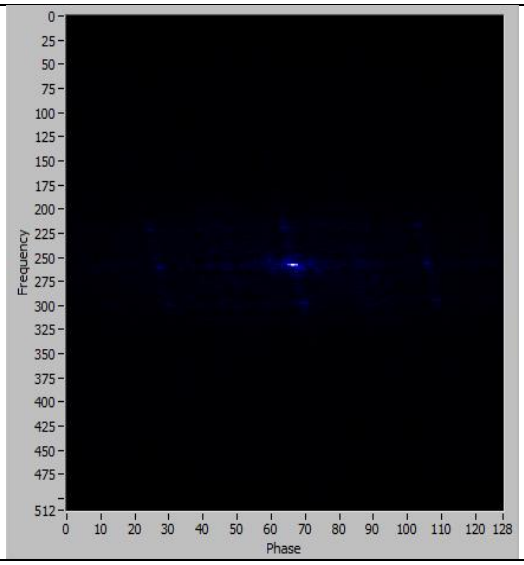
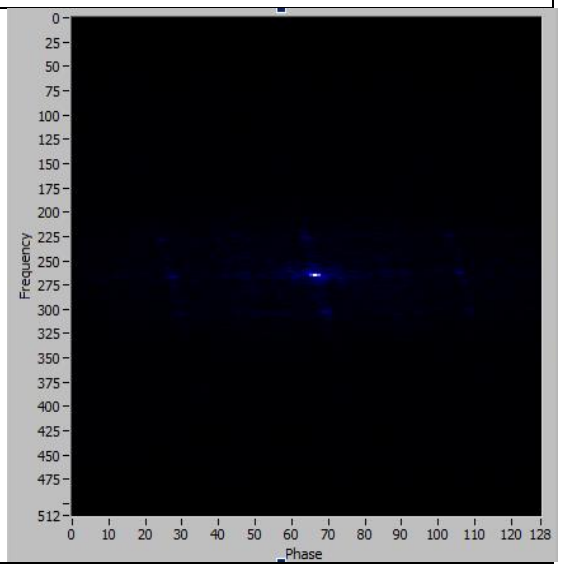
	Pentek Data	Varian Data
K-space		

Figure 45 K-space of Pentek & Varian acquired echo (Phantom with pin cushion)

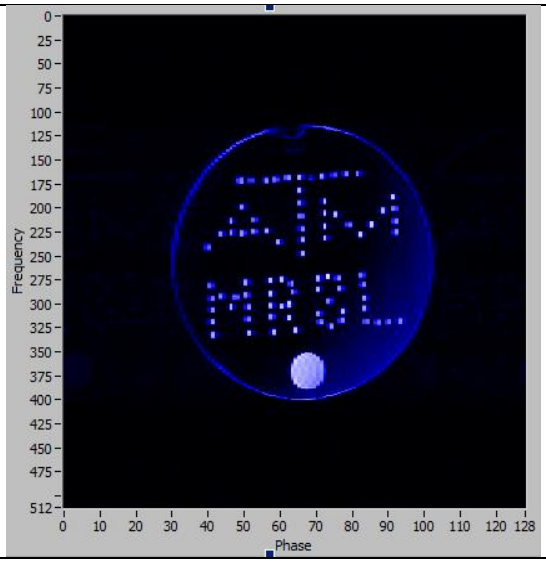
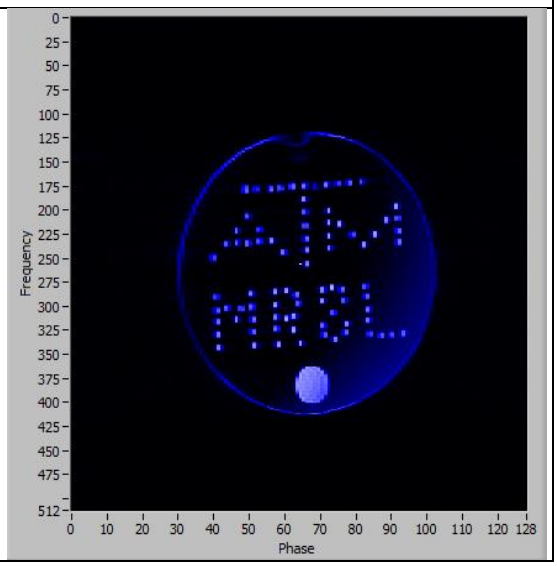
	Pentek Data	Varian Data
Image2		

Figure 46 Image Reconstruction with Pentek & Varian (Phantom with pin cushion)

The rectangular region was selected in image domain to compute signal and noise. The image based on the pin cushion on the left produced SNR of 124.745. and The image on the right computed its SNR to be 128.644.

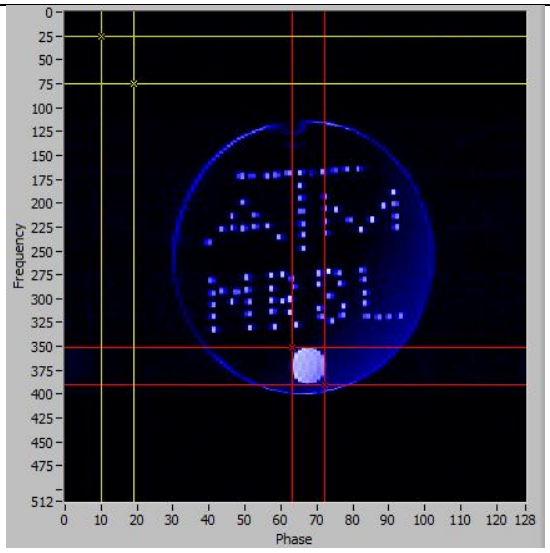
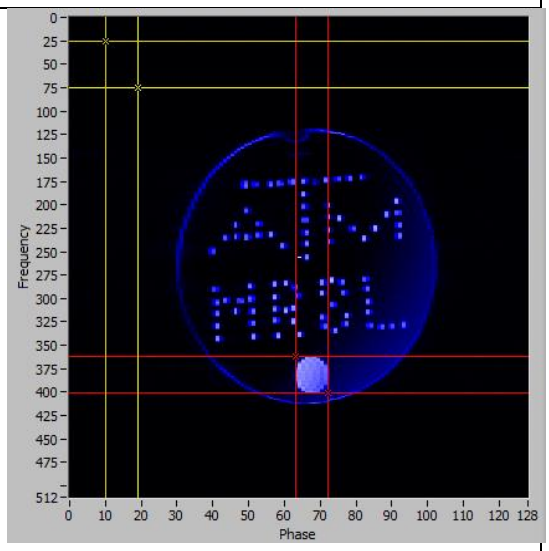
	Pentek Data	Varian Data
Image2	 SNR: 124.745	 SNR: 128.644

Figure 47 SNR comparison of Pentek & Varian (Phantom with pin cushion)

	Pentek			Varian		
	Signal	Noise	SNR	Signal	Noise	SNR
Image 1	7.37499E+8	5.06569E+6	145.587	0.87813	0.00598825	128.644
Image 2	2.57559E+7	206468	124.745	0.759164	0.00590129	128.644

Table 1 SNR comparison - Pentek & Varian

5.2 Simultaneous Nuclei Capture of ^{2}H, ^{2}Na, ^{1}H

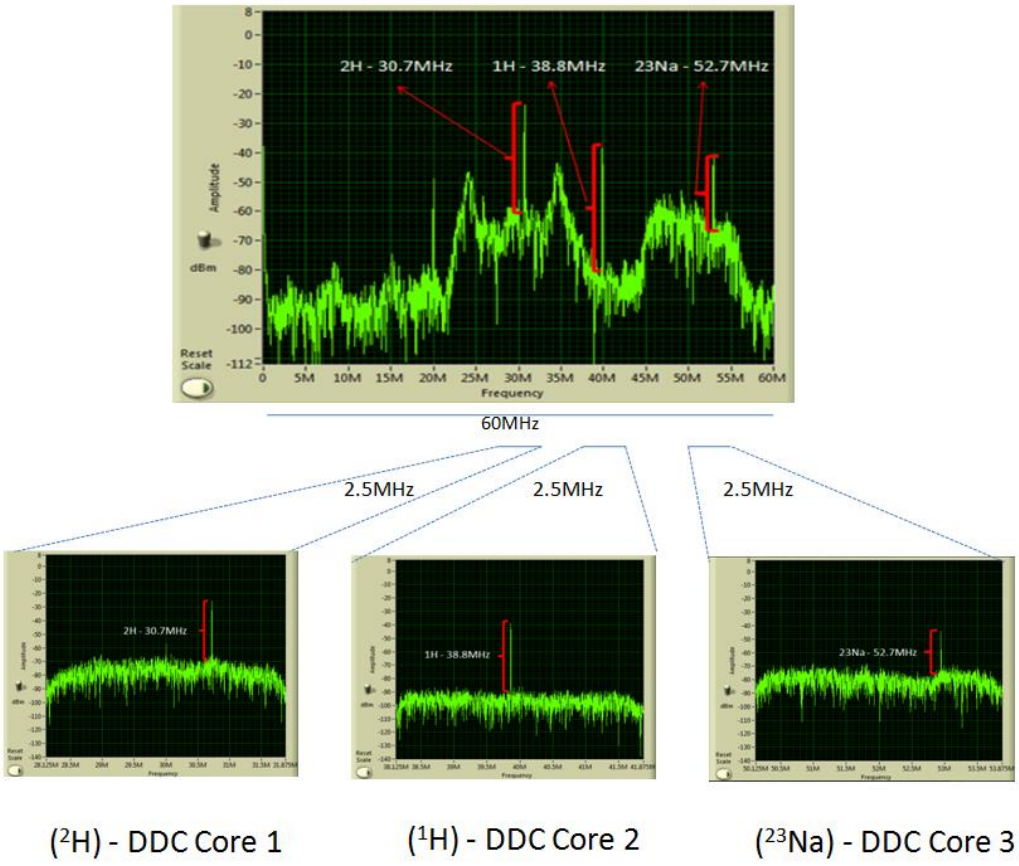


Figure 48 Wideband Capture vs. Narrowband Sub-Channel of ^{2}H, ^{1}H, $^{,23}NA$

Pentek can leverage multiple DDC core operating in parallel for each channel. Each independent DDC cores are tuned to specific frequency band to target different nuclei. The figure shows a signal capture of ^{2}H, ^{2}Na, and ^{1}H utilizing parallel DDC cores for a single channel. 120MHz sample rate of ADC captures aliased ^{1}H signal, at 38.8MHz. And ^{2}H, ^{23}Na signals are captured with sufficed Nyquist Frequency. Each of the DDC core was configured with 2.5MHz narrow band FIR filter. The direct sample would utilizes 60MHz of Nyquist capture bandwidth for 120MHz sample rate. The narrow band sub-channel utilizes bandwidth of 7.5MHz from each

channel configured with DDC. In a field (B_0) of 4.7 Tesla, the resonance frequency of ^{1}H, ^{23}NA, ^{2}H is computed to be 200.112MHz, 52.931MHz, 30.719MHz respectively.

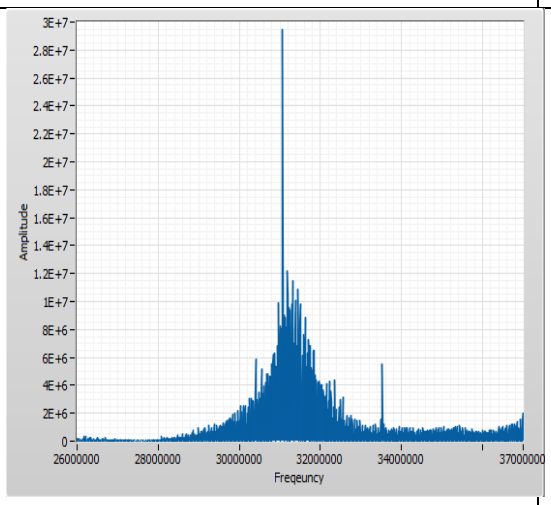
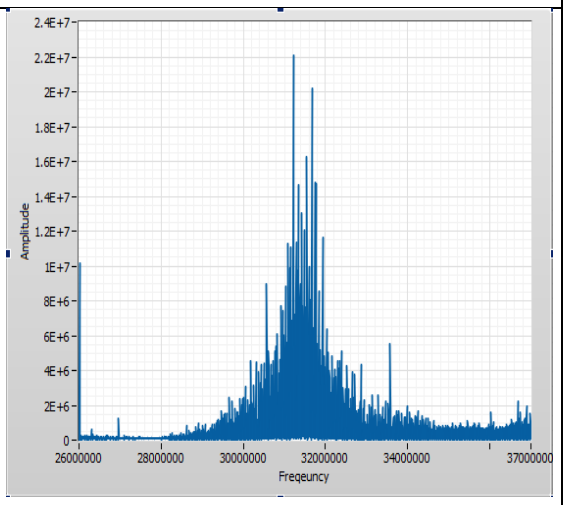
	Pentek Data	Ultraview Data
SNR		
	SNR:67.453	SNR:58.71

Figure 49 SNR comparison of Pentek and Varian for ^{2}H

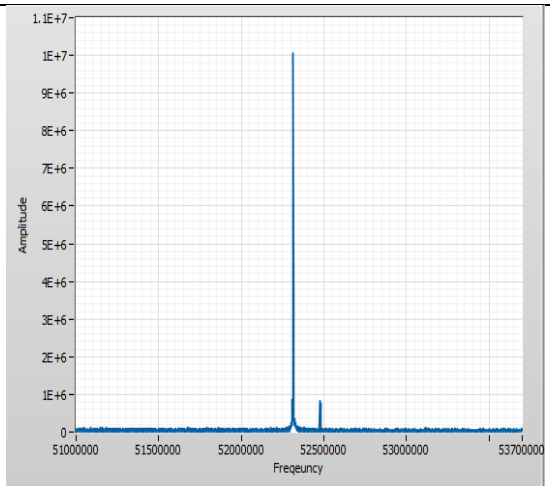
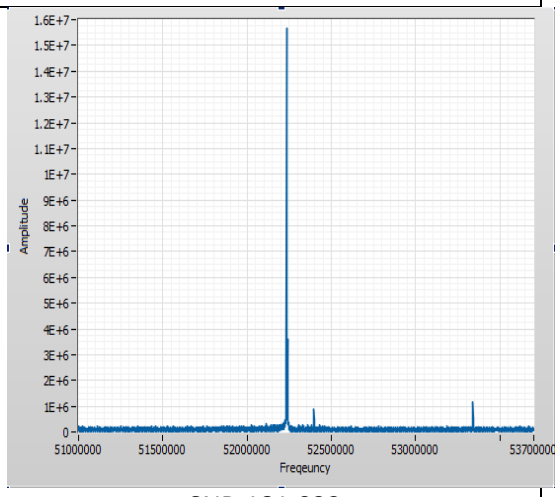
	Pentek Data	Ultraview Data
SNR		
	SNR:162.573	SNR:181.032

Figure 50 SNR comparison of Pentek and Varian for ^{23}Na

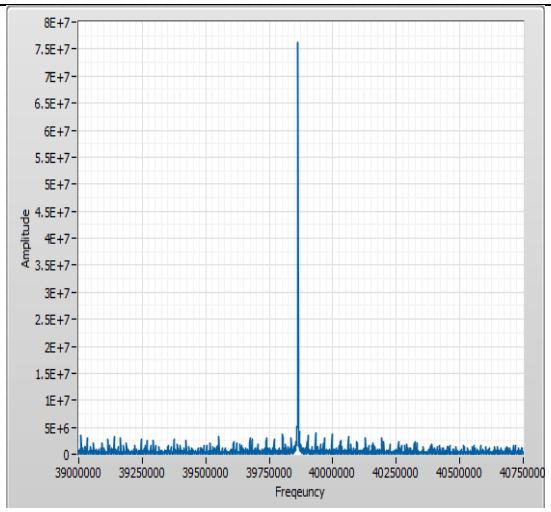
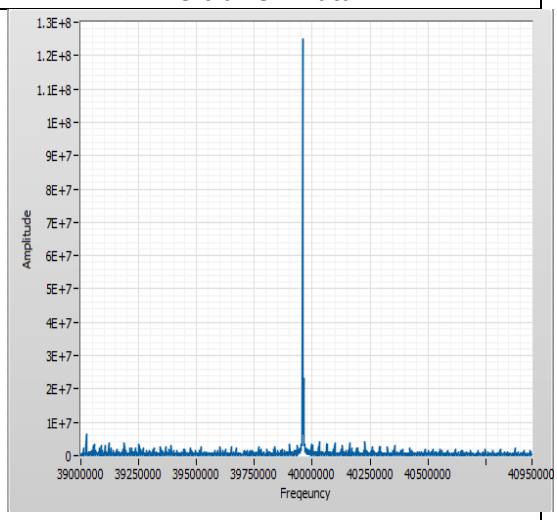
	Pentek Data	Ultraview Data
SNR	 SNR:393.64	 SNR:439.12

Figure 51 SNR comparison of Pentek and Varian for ^{1}H

5.3 ^{31}P Spectroscopy

^{31}P NMR experiment were performed on a 12 cm NMR 1.0T equipment with 4 independent acquisition channel. For ^{31}P Spectroscopy, physiological phantom data was acquired using the same parameters for both the Pentek and Ultraview. Sampling rate was set to 50MS/s to capture the precession frequency existing at 17.23MHz in the spectrum. The acquisition captures a spectra of chemical shift to detect the difference in resonance frequency between Pi (inorganic phosphate), PCr (Phosphocreatine), and ATP-(adenosine triphosphate). The chemical shift between Pi and PCr causes relative magnitude change generating five distinctive peaks in the spectra. We can observe that the difference is 5 ppm for PCr and Pi, referencing PCr at center (0 ppm) in the spectra. The device can also detect three distinctive peak regarding to ATP(adenosine triphosphate) resonance frequency. In this experiment, Pentek utilized 4 second

repetition time for 32 consecutive echo capture. Acquisition time of 0.512s was used in the experiment having 50% of duty cycle in each trigger sequence. 32 FID data was averaged to improve the signal to noise ratio for each channel.

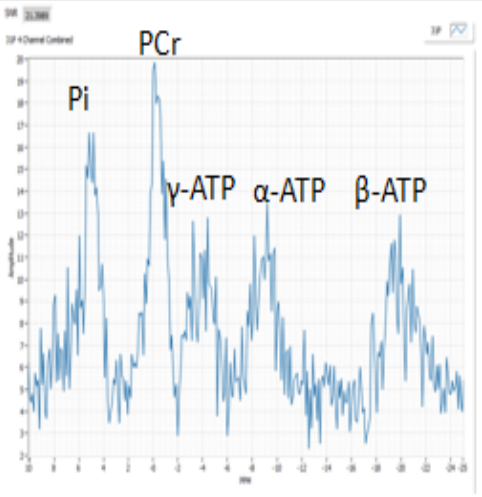
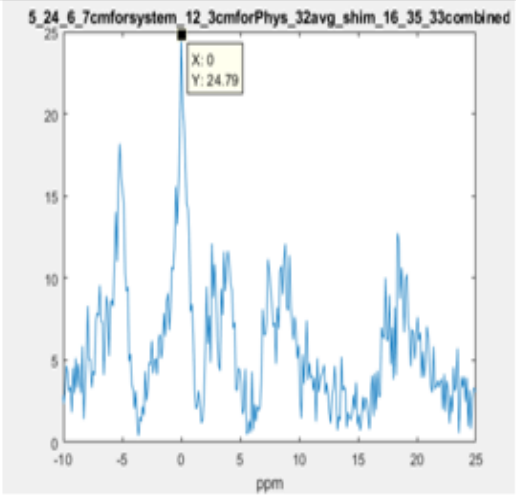
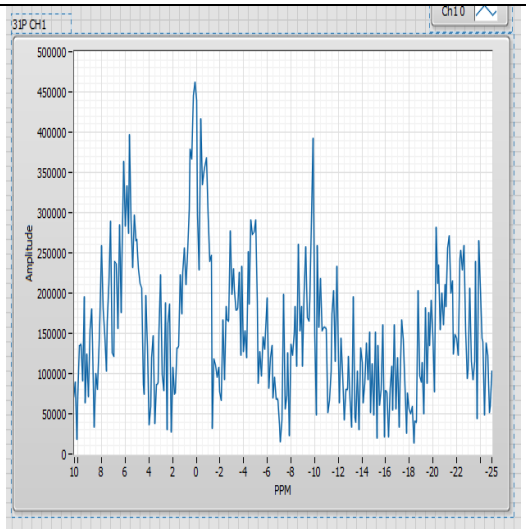
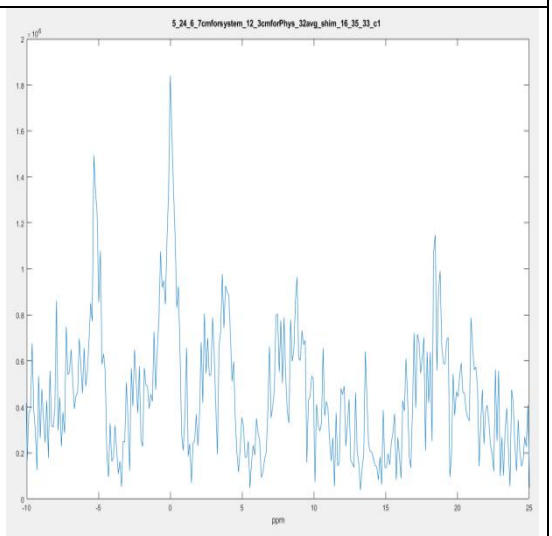
	Pentek Data	Ultraview Data
4 Channel Combined	 combined signal:1598510 noise:74700.42 snr:21.3989	 combined signal:11582139.8666 noise:467260.4418 snr:24.7873

Figure 52 4 Channel combined ^{31}P spectra with 32 averages

	Pentek Data	Ultraview Data
Channel 1	 c1 signal: 461793 noise: 40249.74 snr:11.4734	 c1 signal:1840030.166 noise:111534.2863 snr:16.4974

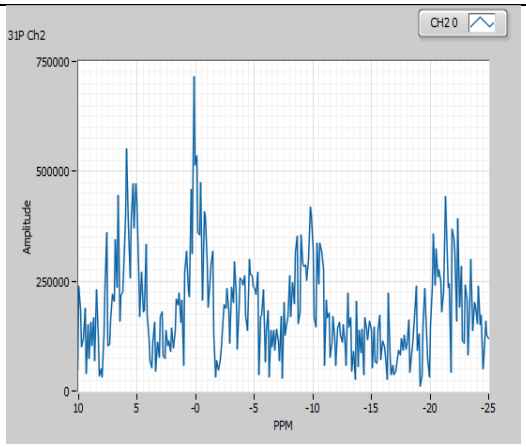
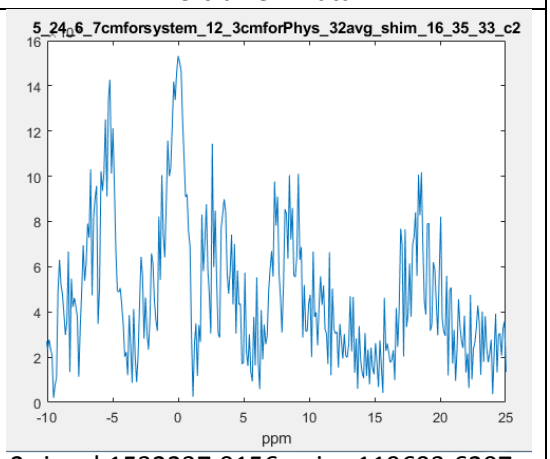
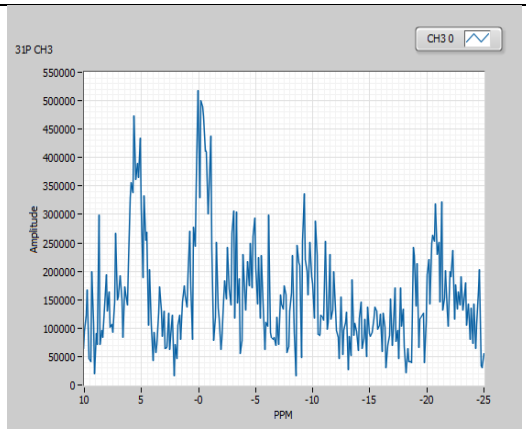
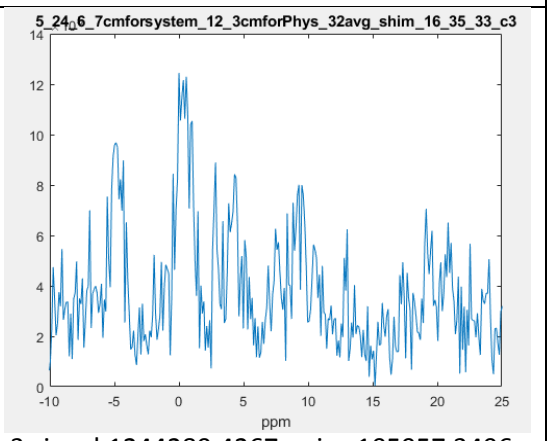
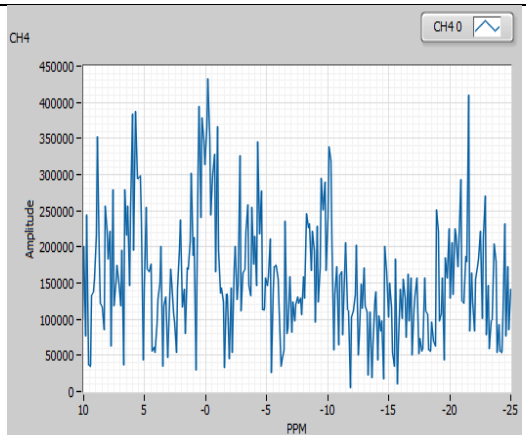
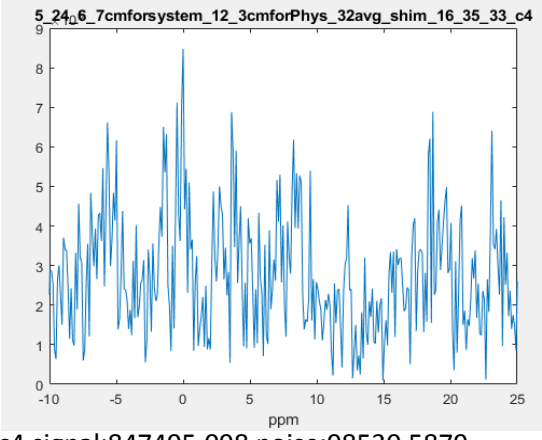
	Pentek Data	Ultraview Data
Channel 2	 c2 signal: 715456 noise: 47806.52 snr:14.9657	 c2 signal:1532237.0156 noise:119693.6207 snr:12.8013
	Pentek Data	Ultraview Data
Channel 3	 c3 signal: 518355 noise: 42911.40 snr:12.0797	 c3 signal:1244289.4267 noise:105957.3406 snr:11.7433
	Pentek Data	Ultraview Data
Channel 4	 c4 signal: 432175 noise: 45257.92 snr:9.54915	 c4 signal:847495.098 noise:98530.5879 snr:8.6013

Figure 53 ^{31}P spectra data of 4 channels (Pentek and Ultraview)

	Pentek			Ultraview		
	Signal	Noise	SNR	Signal	Noise	SNR
Channel 1	461793	40249.74	11.4734	1840030.16	111534.28	16.49
Channel 2	715456	47806.52	14.9657	1532237.01	119693.62	12.80
Channel 3	518355	42911.40	12.0797	1244289.42	105957.34	11.74
Channel 4	432175	45257.92	9.54915	847495.09	98530.58	8.60
Combined Result	1598510	74700.42	21.3989	11582139.86	467260.44	24.78

Table 2 ^{31}P signal to noise ratio 4 channel combined with 32 averages

6. CONCLUSIONS

It was shown in this study that Wideband and Narrowband NMR signal acquisition can be operated through the implementation of DDC core. The Software Define Radio (SDR) device fulfills high processing speed and high data throughput utilizing narrowband FIR filters implemented in FPGA. Decimator logic implement in FPGA IP core allows the system to control the flow of input data stream to the PC, reducing sample points. In this research we have achieved to develop a RF receiver that would handle data input stream with high processing speed. This research work has shown simultaneous nucleus signal capture using direct sampling method and narrowband sub-channel capture method. The system has shown its capability to handle simultaneous nuclei signal capture of ^{2}H, ^{23}NA, ^{1}H with independent DDC core operating in parallel. Direct-Memory-Access (DMA) function implemented in FPGA has achieve to handle multiple input stream of data without overflowing the memory space.

In this research work, we have examined methods in acquisition software to systematically operate implemented FPGA logics through LabVIEW software. Software structure (e.g. State Machine, Parallel DDC logic execution) was design to maximize its performance in parallel processing to organize the device APIs to provide systematic control in the runtime engine. In this work we have developed a RF receiver capable of capturing NMR signal continuously in wide range of frequency band.

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